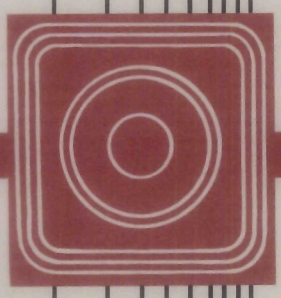
SURFACE MOUNT TECHNOLOGY: A RELIABILITY REVIEW



RAC

Reliability Analysis Center

A DoD Information Analysis Center

Ordering No. SOAR-5

SURFACE MOUNT TECHNOLOGY: A RELIABILITY REVIEW

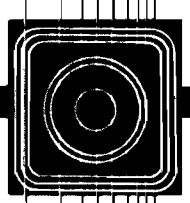
1986

Prepared by:

Susan B. Stockman and David W. Coit
IIT Research Institute

Under Contract to:

Rome Air Development Center
Griffiss AFB, NY 13441-5700



Reliability Analysis Center

A DoD Information Analysis Center

The Reliability Analysis Center (RAC) is a Department of Defense Information Analysis Center sponsored by the Defense Logistics Agency, managed by the Rome Air Development Center (RADC), and operated at RADC by IIT Research Institute (IITRI). RAC is chartered to collect, analyze and disseminate reliability information pertaining to electronic systems and parts used therein. The present scope includes integrated circuits, hybrids, discrete semiconductors, microwave devices, opto-electronics and non-electronic parts employed in military, space and commercial applications.

Data is collected on a continuous basis from a broad range of sources, including testing laboratories, device and equipment manufacturers, government laboratories and equipment users (government and non-government). Automatic distribution lists, voluntary data submittals and field failure reporting systems supplement an intensive data solicitation program.

Reliability data and analysis documents covering most of the device types mentioned above are available from the RAC. Also, RAC provides reliability consulting, training, technical and bibliographic inquiry services which are discussed at the end of this document.

REQUEST FOR TECHNICAL ASSISTANCE AND INFORMATION ON AVAILABLE RAC SERVICES AND PUBLICATIONS MAY BE DIRECTED TO:

Reliability Analysis Center
P.O. Box 4700
Rome, NY 13440-8200

Technical Inquiries (315) 337-9933
Non-Technical Inquiries: (315) 330-4151
Autovon: 587-4151
TeleFax: (315) 336-9932

ALL OTHER REQUESTS SHOULD BE DIRECTED TO:

Rome Air Development Center
RBE/Preston R. MacDiarmid
Griffiss AFB, NY 13441-5700

Telephone: (315) 330-4920
Autovon: 587-4920

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited. Available from RAC or DTIC in microfiche only.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) SOAR-5	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION Reliability Analysis Center 6b. OFFICE SYMBOL (*If applicable*) RADC/RAC	7a. NAME OF MONITORING ORGANIZATION RADC/RBE
6c. ADDRESS (*City, State, and ZIP Code*) Rome Air Development Center Griffiss AFB, NY 13441-5700	7b. ADDRESS (*City, State, and ZIP Code*) Griffiss AFB, NY 13441-5700
8a. NAME OF FUNDING/SPONSORING ORGANIZATION DLA/DTIC 8b. OFFICE SYMBOL (*If applicable*) DTIC-AI	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F30602-84-C-0162
8c. ADDRESS (*City, State, and ZIP Code*) DTIC Cameron Station Alexandria, VA 22314	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. 65802S; PROJECT NO. 1.0; TASK NO.; WORK UNIT ACCESSION NO
11. TITLE (*Include Security Classification*) Surface Mount Technology: A Reliability Review	
12. PERSONAL AUTHOR(S) Susan B. Stockman and David W. Coit	
13a. TYPE OF REPORT 13b. TIME COVERED FROM _____ TO _____ 14. DATE OF REPORT (*Year, Month, Day*) 1986, May 13 15. PAGE COUNT	
16. SUPPLEMENTARY NOTATION Hard copies available from Reliability Analysis Center, RADC/RAC, Griffiss AFB, NY 13441-5700 (Price $56.00) DTIC will provide microfiche copies to the DoD and its contractors at the standard microfiche price. DTIC Source Code: 408944	

17. COSATI CODES		
FIELD	GROUP	SUB-GROUP
11	07	
13	08	

18. SUBJECT TERMS (*Continue on reverse if necessary and identify by block number*)
Surface Mount Technology; Failure Mechanisms; Surface Mount Components; Reliability Modelling; Physics of Failure

19. ABSTRACT (*Continue on reverse if necessary and identify by block number*)

This document is primarily concerned with establishing through investigative analysis the reliability functions of surface mount technology. Highlighted are reliability models for surface mount packaging, solder joint connections and printed wiring boards. Specific failure mechanisms associated with surface mount technology are discussed. The status of surface mounting in the scope of today's manufacturing environment and the immediate concerns of manufacturers/users are investigated. Most of the material presented is universally applicable to different devices and device packages; the emphasis is placed on microcircuit packaging and reliability.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION
22a. NAME OF RESPONSIBLE INDIVIDUAL Kieron A. Dey, RAC Technical Director	22b. TELEPHONE (*Include Area Code*) (315) 330-4151 Av: 587-4151 22c. OFFICE SYMBOL RADC/RAC

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted. All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE

PREFACE

This document is the fifth in a series of state-of-the-art reports prepared by the Reliability Analysis Center. The report's primary purpose is to establish, through investigative analysis, the reliability functions of surface mount technology (SMT).

The report contains investigations on:

- the status of surface-mounting in the scope of today's manufacturing environment
- the immediate concerns of manufacturers/users
- the specific failure mechanisms associated with surface mount technology
- the preparation of reliability models for surface mount packages, solder joints and printed wiring boards

The authors would like to gratefully acknowledge the contributions of the following individuals:

- Gene Blackburn (RADC) and William Denson for reviewing the document and providing technical support.
- Gregory Chandler and Richard Wanner for providing data base support.
- Shawn Gentile for her diligent typing and graphics efforts.
- Gina Nash and Helen Adsit for their moral support.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES
(CONTINUED)

LIST OF ACCRONYMS

SMT - Surface Mount Technology
SMC - Surface Mount Component
SMD - Surface Mount Device
CC - Chip Carrier
CCC(C^3) - Ceramic Chip Carrier
LCC - Leadless Chip Carrier
CLCC - Ceramic Leadless Chip Carrier
LCCC(LC^3) - Leaded Ceramic Chip Carrier
HCC - Hermetic Chip Carrier
PCC - Plastic Chip Carrier
PLCC - Plastic Leaded Chip Carrier
IC - Integrated Circuit
SOIC - Small Outline Integrated Circuit
DIP - Dual-In-Line Package
PCB - Printed Circuit Board
PWB - Printed Wiring Board
PTH - Plated Through-Hole

SECTION 1: THE PACKAGING REVOLUTION

The objective of this document is to present an overall picture of surface mount technology (SMT) by establishing its roots, providing some insight into its complexities and exploring its reliability. The scope is primarily a reliability review of surface mount packaging, solder joint connections and printed wiring boards. Most of the material presented is universally applicable to different devices and device packages; however, the emphasis is placed on microcircuit packaging and reliability.

Surface mount technology differs from the customary through-hole assembly of electrical devices by soldering the components directly to metallized pads or footprints on the surface of the printing wiring board (PWB). Comparably, conventional DIP technology consists of inserting the wire leads of components through plated holes which have been drilled in the board. The solder joint of a surface-mount component (SMC), therefore, serves as both an electrical and a physical connection to the PWB. Since surface-mounting eliminates the need for hole-drilling to accomodate component leads, these smaller-dimensioned components can be placed closer together and on both sides of the board. This contribution releases valuable board real estate for more component placement or simply reduces overall board size.

The trend in the semiconductor industry toward increasing circuit integration is being accompanied by advances in packaging techniques, and both are designed to increase the performance and to reduce the size, weight and cost of high-package-density electronic assemblies. Competitive pressures and advances toward miniaturization for virtually all system designs are the motivating factors influencing this revolution; and since the technological arena often finds that the major burden of effective competition lies in significant cost savings, the use of surface mount technology is indeed enticing -- or is it?

The heading from an article which appeared in an electronics trade magazine reads "SMCs Invade Military and Commercial Equipment" (Ref. #1) and the message is clear: watch out! The article conveys a theme of serious consideration for this prospective advance and declares that certain victory lies in store for those who choose to participate. It follows that SMT, promoted as an approach which will prove to be one of the most economical methods for electronic assembly, is also embraced as a mechanism necessary for any manufacturer/user who plans to be a viable contender for future business opportunities. An attitude prevails through this hi-tech community of an urgent need to become more than just familiar with surface-mounting and to make this move which is deemed essential for economic survival.

The following military electronics programs (all at varying stages of development) have adopted SMT and are actively engaged in implementing these new configurations. Table 1 presents these equipments and their relative stages of development.

To date, all field experience attests to the successful implementation of SMT as a viable manufacturing technique. Tracor Industries (Ref. #2) claims that the following systems using thick film substrate assemblies have operated in the field for the past two years without failures attributable to either the SMT packages or the substrates. These systems, including aircraft, land vehicles/backpacks and submarines, contain either a GPS/NAVSTAR CPU assembly for use in the Receiver/Processor User Equipment or a MIL-STD-1750A processor for use in the AN/APG-67 Radar System:

F-16 Aircraft
C-141 Aircraft
F-20 Tigershark (1750A)
M-35 Truck
M-60 Tank

TABLE 1:

MILITARY PROGRAMS USING CHIP CARRIER TECHNOLOGY

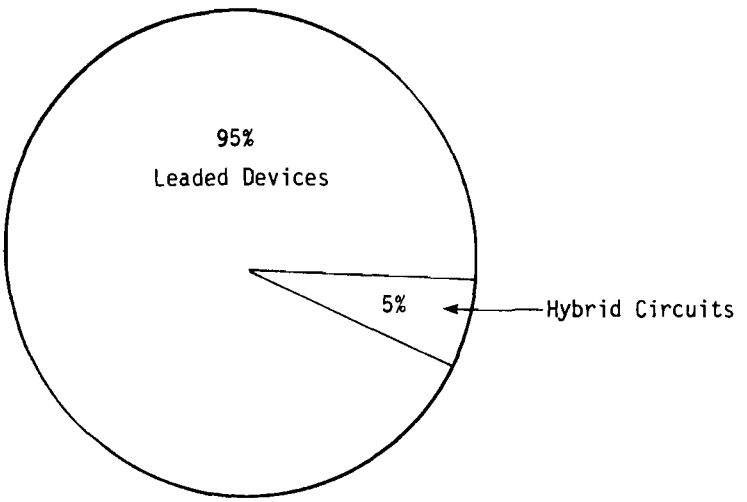
DEVELOPMENT PHASE	PREPRODUCTION PHASE	PRODUCTION PHASE
F20 Radar	EDM 4-Navy Radar	UYK/44-MIL Computer
Augusta-Helicopter MU	JTIDS-F15 Info Sys	F15-Countermeasures
GPS-Global Pos Sys	AMRAAM-Missile	SEM-Standard Module
EMPS-Signal Proc	Subacs-ASW Combat	B1B-Defensive Avionics
AVCAP-Advanced Cap	BIU-Buss Interface	F16-Radar Module
MILSTAR-Grnd Support	UCG-Unit Controller	FMS-FLT Comp
Gulfstream-A/C Nav	ELF-Sub Communication	
Lantirn-IR Guidance	SADS-Sonar Det Sys	
Taflir-Memory Board	Trident 11-Fire Contr	
Digiscan-Display	Cobra-Display	
MRT-Revr/xmtr	TPS70-Radar Memory Brd	
Matcals-Marine ATC	EA6B-Countermeasures	
Bancroft-Radio	Sidewinder-Missile	
Minuteman	Sincgars-Grnd/air Radio	
Seafire		
Cains 11-Missile Guidance		
LN20-Missile Guidance		
Majic 5-FMS		
Aquila-Drone		
CVLF-Radio		
Lamps-Radar		
Seamag-Missile Guidance		
ALQ-149 Countermeasures		
Madar-Comp, Mem Board		
ALQ99-Countermeasures		
DMGF-MPA Generator		
AINS-Missile Guidance		

The Rockwell International Corporation has utilized leadless electronic components since the late 1970s. The leadless chip carrier/polyimide PWB assemblies, designed for high-performance aircraft applications, have utilized 80,000 printed circuit boards populated with more than 4 million chip resistors/capacitors and 75,000 ceramic leadless chip carriers. The documentation indicates that the reliability has been found to be in excess of the design requirements by 30 percent (Ref. #3).

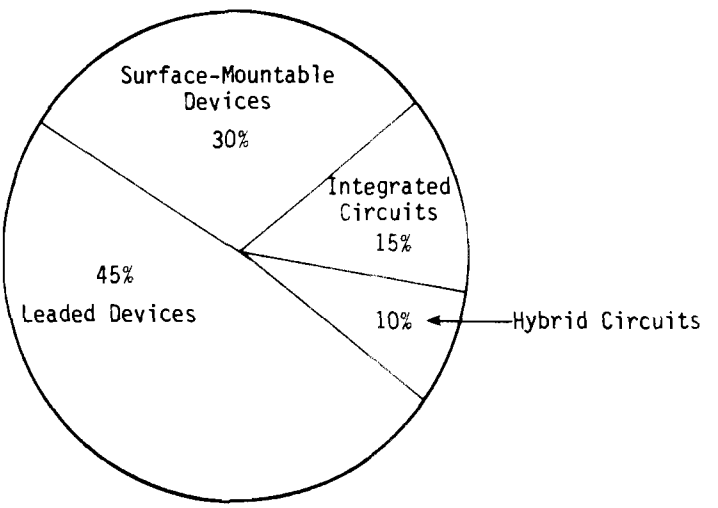
North American Philips SMC Technology Inc., Milwaukee, WI, considered an industry leader in the utilization of SMT, contends that this emerging technology can boast increased productivity, reduced production costs and improved reliability. Figure 1 establishes the past, present and future impact of SMT on the microcircuit industry as viewed by North American Philips (Ref. #4).

Even the "Wall Street Journal" heralded the trials and tribulations of SMT in a recent report and drew the inevitable conclusion that this "Improved Circuitry Technique Is Coming Into Its Own at Last" (Ref. #5).

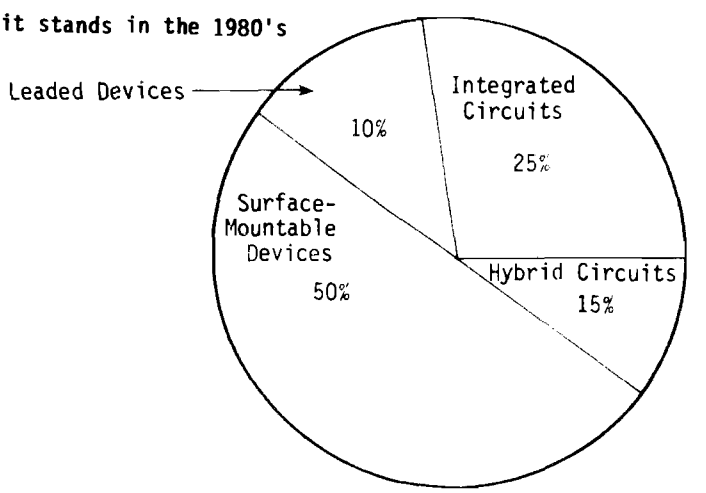
However, there is also an underlying conservative pressure which is begining to build in an attempt to slow this pace, suggesting that there is a need to reevaluate its significance and to verify the benefits and the pitfalls of SMT. The concept of packaging can no longer be considered a stable element in current designs but a dynamic part of the system, and therefore the successful introduction of surface mount components has given rise to requirements for the simultaneous development of new circuit designs, manufacturing equipments and assembly techniques.



How it was in the 1950's



As it stands in the 1980's



What is expected in the year 2010

FIGURE 1:
THE PAST, PRESENT AND
FUTURE IMPACT OF SMT

PAGE 29
FRIDAY, SEPTEMBER 13, 1985

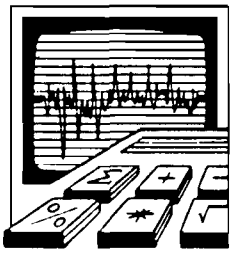
THE WALL STREET

TECHNOLOGY

Improved Circuitry Technique Coming Into Its Own at Last

IN THE ELECTRONICS INDUSTRY'S constant quest for lower costs and more compact products, any technique that halves production costs and crams twice as much circuitry into the same space would seem to be an overnight success.

Not so with surface-mount technology, which was first used in making digital watches in 1975. Only a tiny fraction of computer equipment uses surface mounting, including a few disk drives introduced this year. High equipment costs, a lack of a standard approach and industry resistance to change have hampered its adoption.



But now the technique is starting to come into its own and, according to some forecasts, will become a mainstay in making everything from personal computers and TV sets to cameras and phone-switching systems. Texas Instruments Inc. expects half or more of all memory chips to utilize it by 1989, compared with 7% this year. Gnostic Concepts, a San Mateo, Calif., forecasting concern, says surface-mounted circuitry will be used in 27% of electronics equipment by 1988, up from 10% or so this year.

THE TECHNIQUE IS an alternative to wiring circuits on the boards inside electronic products by the "through-hole" process that manufacturers have typically used. In the through-hole process, makers attach parts to boards by ramming "leads," or wires, through pinhead-sized holes and then soldering the leads to copper "traces," which are the wiring pathways on the underside of the board that carry electrical signals from circuit to circuit. The process requires elaborate, costly precision to drill the hundreds or thousands of tiny holes and manipulate the wires and soldering.

In surface-mount technology, parts are soldered directly to traces laid out on the surface of the board. The holes, wire leads and complex routing are eliminated. Moreover, a surface-mount board, which unlike a conventional board can carry parts on both its sides, can hold four times as many parts as a similar-sized board assembled under the older process.

The result is cheaper, lighter, smaller and more sophisticated computers. Just eliminating the drilling saves one to three cents per hole, says William H. Bullen, a Texas Instruments manager. He says one prototype computer board, for instance, is 58% smaller and 50% less costly because of a switch to surface mount.

—DENNIS KNEALE

Early applications of surface-mounting techniques were primarily in areas such as military electronics, but in recent years the consumer electronics portion of the industry has been reshaping the market. The higher initial investment for incorporating SMT is generally a major stumbling block for commercial markets, a factor less apparent to military concerns. Today, strong emphasis exists in high-reliability military equipments, data processing and telecommunications, but the size-reduction aspects alone have become important in non-military applications such as consumer electronics, computers and automobiles. Surface-mounting has been exploited by the Japanese with great success since the mid 1970s specifically in their consumer electronics markets, claiming significant cost savings and performance advantages over traditional packaging styles. The Japanese focus has been on discrete chip components and leaded LSI devices, directing that concentration toward effective packaging for thin calculators and watches. The high-volume users in the automotive industry have recently been joined by a second wave of users in the areas of telecommunications, instrumentation and peripherals. It is now apparent that a third wave is being composed of small-to-medium-size users who are influenced by the space-savings, reliability and lower assembly costs.

A current profile of the electronics industry indicates that the major equipment markets driving this technology are influenced by three basic factions: the military, the high-performance mainframes and the commercial high-volume equipments. Figure 2 describes the relationships involved between the major forces motivating the industry toward SMT (Ref. #6).

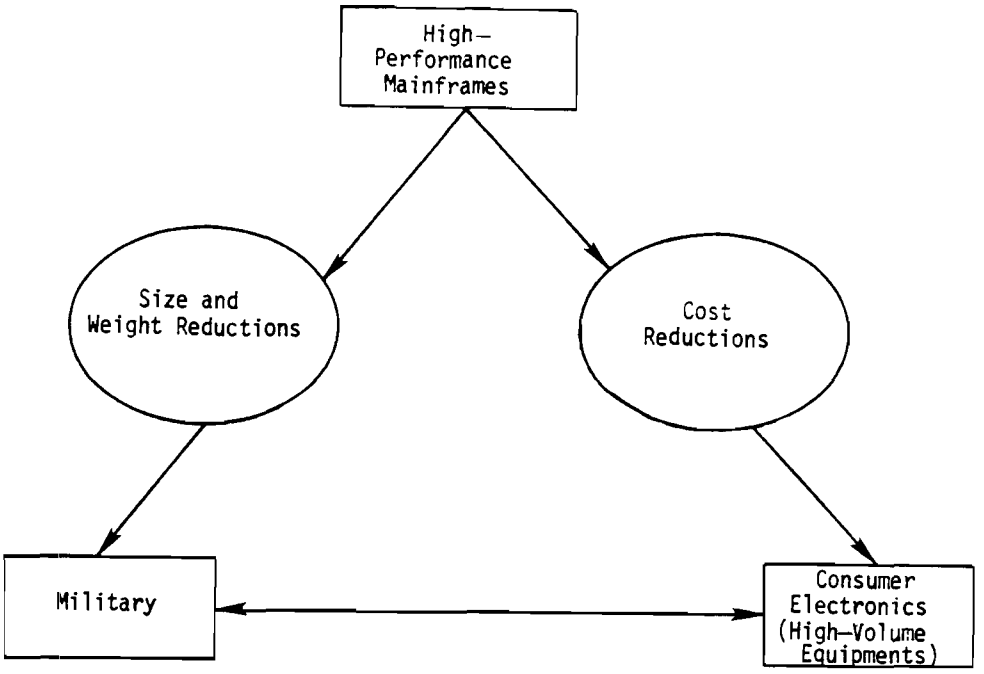


FIGURE 2:
THE MAJOR MOTIVATING FORCES BEHIND SMT

Figure 3a shows comparative printed wiring board areas utilized by various package styles. This presentation of area comparisons for various package styles is by no means complete but rather it is meant to represent the relative differences between traditional packaging and surface mount packaging. The chart is also provided to indicate the levels at which packaging schemes change; that is, DIPs are available from 4 to 64 pins. Beyond the 40-pin point, DIPs are generally considered inefficient. Small-outline integrated circuits (SOICs) range from approximately 8 to 28 pins, at which point they begin to lose their attractiveness. At 16 pins, the chip carriers are introduced to become a viable alternative for medium to very-large-pin-out requirements. The functional circuit board complexity (total circuit gate count) is increased by incorporating more logic into each IC and by utilizing more of these high-density chips in a given circuit board area. Figure 3b shows the impact (for two specific circuits) of increasing pin counts on board area. The graph shows a dramatic reduction in the number of ICs required to accommodate a given number of gates by raising package pin-counts (Ref. #7).

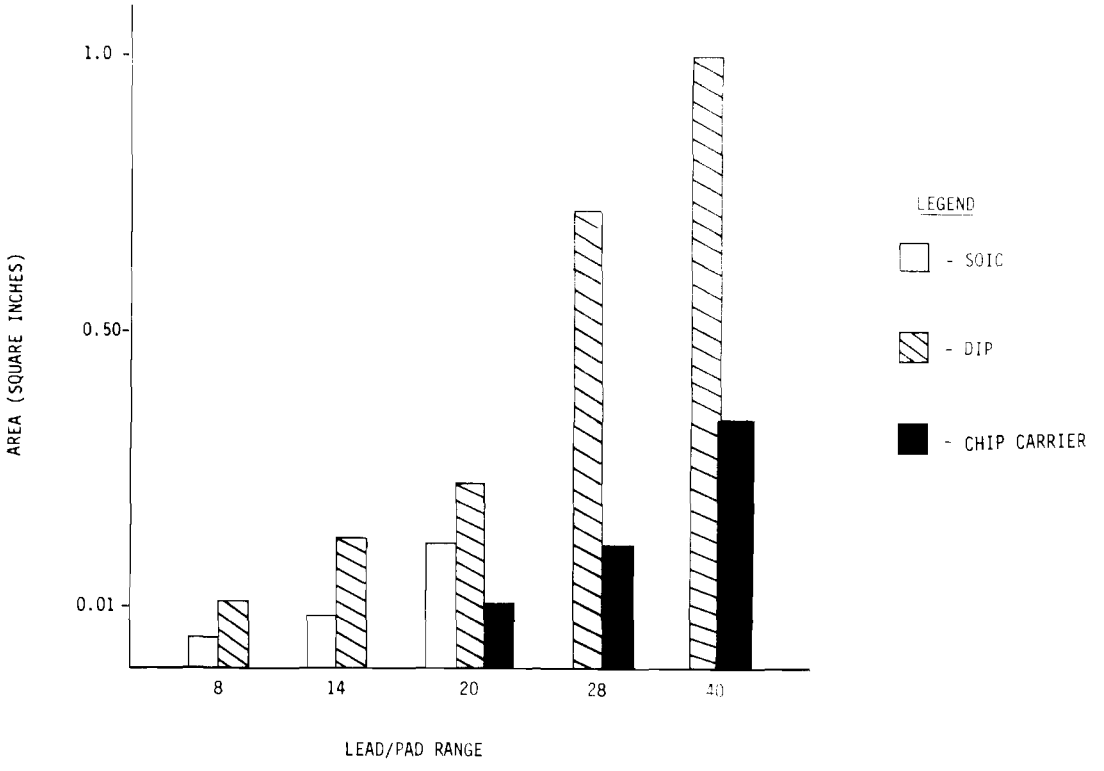


FIGURE 3a:
PACKAGE AREA COMPARISONS

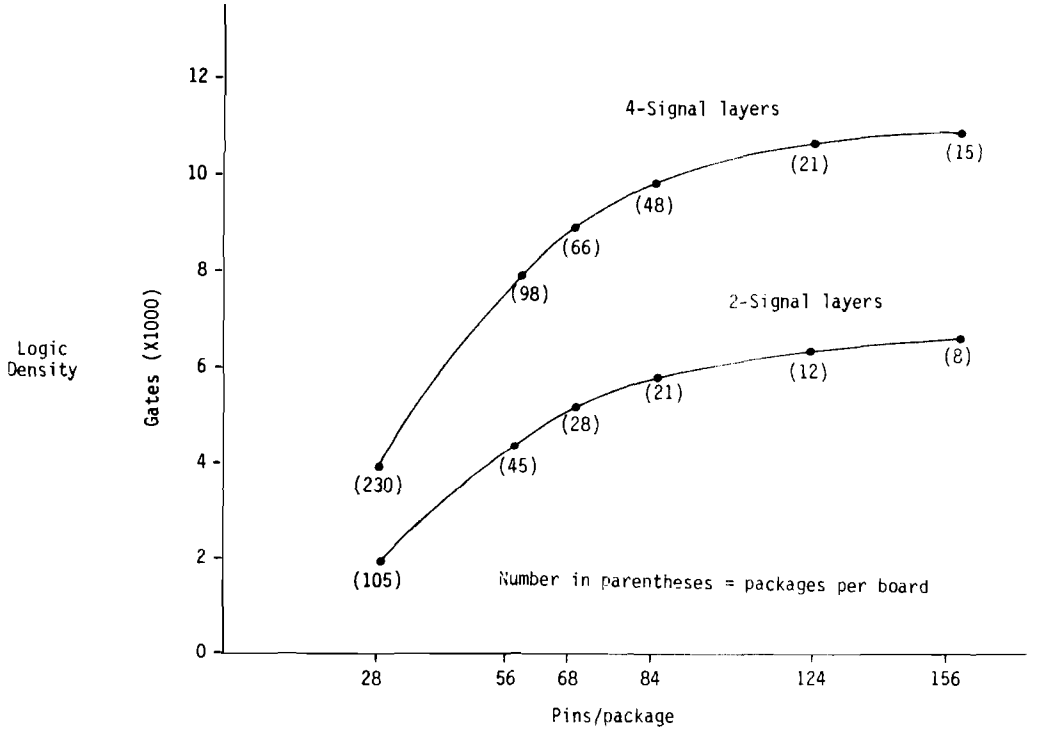


FIGURE 3b:
ACHIEVABLE GATE COUNT FOR A GIVEN
AREA VS. THE NUMBER OF PACKAGE PINS

The high-performance operating parameters and large input/output (I/O) pin counts associated with today's large-scale integrated circuits (LSI, VLSI, VHSIC) are driving conventional dual-in-line packages (DIPs) out of the competition. The DIP, dominating the industry for the past twenty-five years, is being challenged by new packaging and interconnection design requirements. This diversification may not be apparent at first glance, however, because DIPs still account for the majority of integrated circuit packages and, typically, the cost of surface mount components is at a premium compared to standard devices. Proponents of SMT see indirect savings due to higher-density boards and lower overall system costs. This factor coupled with increasing demand will ultimately make these devices cost-competitive with conventional components.

The DIP was developed and became standardized at a time when integrated circuits (ICs) were relatively simple, requiring few I/O connections. The failure mechanisms associated with the DIP have been well-documented and studied, resulting in adjustments and refinements in material selection and assembly processing procedures. The DIP has proven to be a reliable package style that has more than adequately met the demands placed upon it. However, beyond the need for a functional and reliable component is an increasing need for contributions to space efficiency and design flexibility which the DIP is increasingly unable to meet. As the complexity of the ICs increase and the number of leads increase accordingly, the size of the DIP quickly becomes unmanageable and inefficient. Large DIPs (packages requiring 40 pins or more) occupy excessive board area which reduces chip performance due to long connections from the internal die to the external package-to-board terminations. At higher lead counts, the utilization of the DIP begins to diminish the benefits of miniaturization in circuit integration because the packages are utilizing volumes much larger than the chips themselves. Surface mount components have been introduced as the medium to accommodate the size constraints and high-performance capabilities of today's integrated circuits. SMCs do have limitations of their own, however. Even though they have eliminated some of the problems associated with large conventional packages, they have not accomplished the task without introducing some new problems.

The product density evolution can be characterized by three basic increases in assembly design (Ref. #8):

(1) Initially, the general use of small leaded discrete components (resistors, capacitors and transistors) coupled with a few DIPs could achieve a packaging density of 20 components per square inch of board space. The density was derived from close component-placement and two-sided PCB application.

(2) The second evolution was achieved through the use of hybrid ceramic modules whereby the component density rose to approximately 50 components per square inch. This density was achieved by the direct attachment of IC die to the hybrid substrate.

(3) State-of-the-art density is accomplished by the utilization of a wide variety of surface-mountable passive and active components which boosts the range to hundreds of components per square inch of board area.

Other benefits associated with SMT include less parasitic capacitance, lead resistance and inductance (due to shorter lead lengths), plus reduced signal noise and crosstalk especially critical in some high-frequency and linear circuits. Table 2 describes the electrical performance characteristics which can be obtained from leadless components (Ref. #9).

In current electronic equipment designs the successful use of active components (ICs) in surface mount applications is leading the way for their passive-component counterparts. Passive components such as capacitors, resistors, potentiometers, filters, etc., are all being introduced in surface-mountable packages. This development also reiterates the philosophy of proponents of this technology in that there appears to be no benefit in mixing mounting technologies. It is beneficial to either fully invest and convert or remain conventional.

TABLE 2:

CERAMIC LEADLESS CHIP CARRIER

PACKAGE PARASITICS

Pin Count	Size	Trace Resistance (ohms)		Line-to-Line Capacitance (pfd)	
		Short	Long	Short	Long
16	.180 x .180 in.	.108	.114	.184	.232
24	.335 x .335 in.	.136	.139	.228	.164
40/48	.500 x .500 in.	.109	.147	.193	.310
64	.700 x .700 in.	.222	.222	.425	.425

SECTION 2: SURFACE MOUNT PACKAGES

The lack of standardization of package style appears to be limiting the growth potential of this technology. Though there is an eminent need to define package parameters consistent with the philosophy of surface mount techniques, there are some basic requirements which any packaging style must reflect. First, in the case of ICs, the package is responsible for providing the electrical connection between the internal die and the exterior circuit path. A path must also be provided for heat dissipation. The lack of a good path for the heat to escape creates a potentially hazardous operating situation. The package must also be able to provide an interior environment compatible with the device's performance and reliability parameters, and also the package must be strong enough to permit the entire structure to withstand the stresses occurring during manufacturing, assembly, test and actual use.

To ensure general acceptance, future microcircuit packages must provide the following attributes:

- Versatility
  - Variable lead count
  - Compatible with all die attach/interconnect methods
  - Capable of high-speed signal transmission
  - Rugged, small and light-weight

- Readily Available
  - Simple design
  - Easy customization
  - Fast production turn-around
  - Easily shipped, stored and handled

- Cost-Effective
  - Low cost
  - Mass handling/automatic handling
  - Use of existing manufacturing/processing technology
  - Function as a simple or complex package

- High Reliability
  - Electrical and environmental characteristics consistent with design requirements
  - Compatible package-to-board interconnect thermal coefficients of expansion (TCE) characteristics to eliminate unwanted interface effects
  - Encapsulant material must be a good thermal conductor
  - ESD-protected

General Characteristics of Surface Mount Components

The first generation of integrated circuits were constructed as DIPs with 100-mil centers. The second generation ICs were the Small-Out-Line ICs (SOICs) and chip carriers (CC) with 50-mil centers. Today the industry is considering the third generation of ICs to accomodate pin counts in the 124 to 300 range on diminishing center spacings.

Surface mount components have either very short leads or no leads at all. They are generally produced on 0.050" lead centers. However, designs do exist on 0.040", 0.025" and 0.020" lead centers. This spacing refers to the center-to-center spacing width between adjacent leads and is referred to as "pitch." This is a major design change from the tradtional 0.100" center spacing of DIPs, a change which allows many more leads to be utilized on a package of similar dimensions.

The Joint Electronic Device Engineering Council (JEDEC) is a well-recognized purveyor of standards for the electronics industry. These standards define various styles and sizes of both leadless and leaded packages. Table 3 presents a summary of chip carriers currently in the market.

Table 4 presents the JEDEC designations for the standard 50-mil center chip carrier family along with descriptions, illustrations, electrical connection points and remarks (Ref. #7).

TABLE 3:

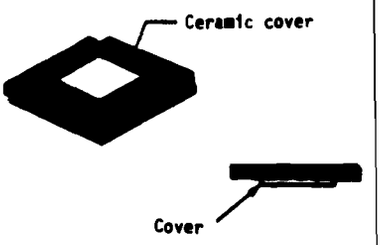
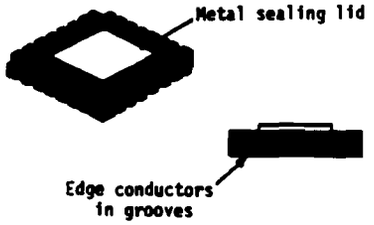
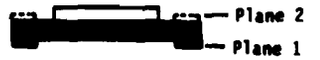
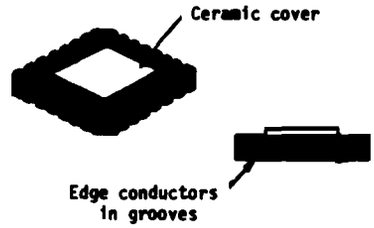
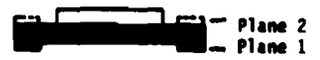
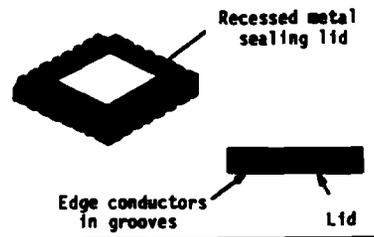
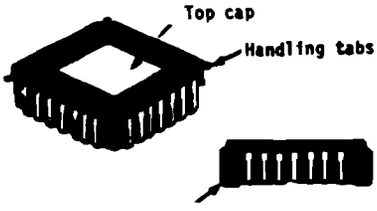
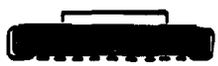
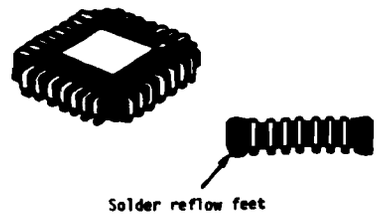
CHIP CARRIER AVAILABILITY BY PIN COUNT

Overall Dimension of Square Packages	Center-to-Center Lead Spacing			
	.050"	.040"	.025"	.020"
0.235"	-	16*	-	-
0.300"	16	20	28	36
0.330"	-	20*	36	44
0.350"	20*	24*	36	48
0.400"	24	28	44	60
0.420"	-	32*	44	60
0.450"	28*	32	52**	68**
0.480"	-	40*	60	76
0.560"	-	48*	68**	92**
0.650"	44*	52	84**	108**
0.720"	-	64*	92	124**
0.750"	52*	64	100**	124
0.920"	-	84*	124	164
0.950"	68*	84	132**	164**
1.040"	-	96*	148	188
1.150"	84*	104	164**	204**
1.350"	100*	124	196**	244**
1.650"	124*	152	244**	308**
2.050"	156*	192	-	-

*JEDEC Standard

**Proposed JEDEC Standard

TABLE 4: JEDEC 50-MIL CENTER CHIP CARRIERS

Type Designation/Description	Illustration	Electrical Connections	Remarks
MS002 0.050" Center, Leadless Type A		 Plane 1 optional Plane 2 required	1. Intended for socket 2. Notches identify as socket version only 3. Single or multiple layer construction 4. Used cavity down for heat dissipation from plane 1, with or w/o a heat sink
MS003 0.050" Center, Leadless Type B		 Plane 1 required Plane 2 optional	1. Intended for sockets or direct solder 2. Single or multiple layer construction 3. Notched configuration for socket compatibility
MS004 0.050" Center, Leadless Type C		 Plane 1 required Plane 2 optional	1. Intended for direct solder; socketing is not recommended 2. Single or multiple construction
MS005 0.050" Center, Leadless Type D		 Plane 1 optional Plane 2 required	1. Intended for socket or direct solder 2. Used cavity down for heat dissipation from Plane 1, with or w/o a heat sink 3. Notched configuration for socket compatibility
MS007 0.050" Center, Leaded Type A			1. Intended for sockets or direct solder 2. Premolded and post-molded versions
MS008 0.050" Center, Leaded Type B		 Plane 1 required Plane 2 optional	1. Leadless Type A with clips for direct solder attach 2. Generally used cavity down with heat dissipation from Plane 1 with and w/o heat sink 3. Single or multiple layer construction

Package Characteristics and Configurations

Surface mount components can be packaged in a number of different styles. The following characterizations identify the package shape and lead style. Also typical designations for each package type are given:

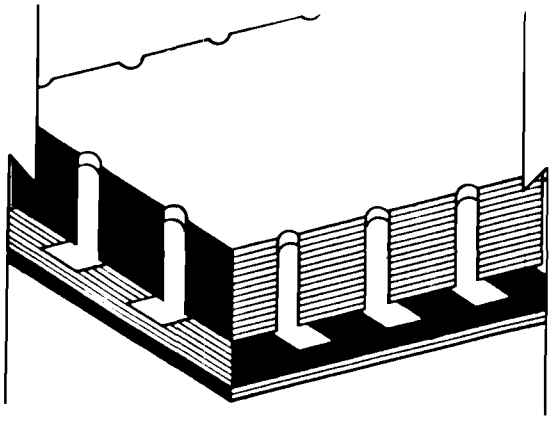
Leadless Chip Carrier - Square or rectangular-type package with fillets or pads on all sides that are used for direct contact to metallized footprints on the printed circuit board. Leadless chip carriers are traditionally ceramic, and the method of mounting the component to the substrate is by direct solder attachment.

The ceramic chip carrier is usually constructed from a 90% to 96% alumina or beryllia base which is bonded with a metallized frame which forms the leads or bonding pads. This process, originally developed for the DIP, forms a rugged structure that resists separation during temperature cycling. The advantage of using these base materials is found in their ability to minimize flexure and to dissipate heat. The metallization is generally a trimetal combination of a refractory metal (such as tungsten or molybdenum), nickel and gold.

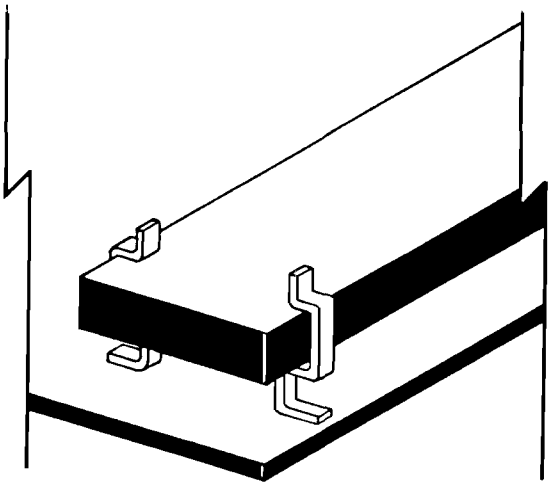
These devices are referred to as **LCCs (Leadless Chip Carriers),** or **CCCs** or **C^3 (Ceramic Chip Carriers),** or **CLCCs (Ceramic Leadless Chip Carriers).** See Figure 4a.

Leaded Chip Carrier - Square or rectangular-type package with leads extending from all sides of the package capable of supporting the package off the surface of the printed circuit board.

Ceramic leaded packages are generally reserved for use in military applications, whereby a ceramic leadless package is transformed into a leaded package by brazing the leads to the sides, top or bottom of the package. Another method which may be utilized to convert leadless packages to leaded ones is through the use of compliant edge-clip mounts. These packages are referred to as **LCCs (Leaded Chip Carriers)** and **LCCCs** or **LC^3 (Leaded Ceramic Chip Carriers) and CLCCs (Ceramic Leaded Chip Carriers.** See Figure 4b.



Leadless Chip Carrier



Leadless Chip Carrier
with Edge-Clip Mounts

FIGURE 4a and 4b:
CHIP CARRIER PACKAGE CONFIGURATIONS

The **Plastic Leaded Chip Carrier (PLCC)** was developed primarily for commercial, industrial and consumer-related applications. There are two types of plastic chip carriers: premolded and postmolded. Both types are composite metal/dielectric assemblies that include a conductor lead frame and a molded insulating body. The premolded chip carrier has one or more apertures for mounting microelectronic elements, while the postmolded chip carrier is a complete assembly without apertures. Leaded devices are generally considered to be mechanically compliant since the leads provide isolation from the different thermal expansion properties of the package and the board. The major benefit in using this package style is the temperature-tolerant characteristics which cause it to be more compatible with conventional printed circuit board materials, since the thermal coefficients do not need to be so closely matched.

The PLCC's lead frame extrudes leads which extend down beneath the package body in the form of a J or out-and-away from the body to form S-shape or Gull Wing leads. See Figures 4c, 4d and 4e. The first type of lead extends down from the package side and bends under the package at the printed circuit board surface in the shape of a J; aptly, they are referred to as J-Leads, J-Bends, J-Hooks, etc. A subtle difference exists between the J-Lead styles even though the terms are often incorrectly used interchangeably from one reference to another. The J-Lead chip carriers are constructed with two basic lead styles. The first configuration is considered a compliant-type lead. The lead is bent at a 90-degree angle under the package at the board interface where it becomes soldered to a metallized footprint. The other type, considered non-compliant, describes a lead that bends at the board surface and turns back up to be attached to the package's underside. The difference between the two is considered critical due to the inability of the non-compliant lead style to withstand numerous thermal/power cycles, contributing failure characteristics similar to those of leadless chip carriers. The failure mechanisms specific to package lead formations is discussed in depth in Section 5.

The use of the J-Lead package styles have advantages and disadvantages which are listed below:

Advantages

- Proven process
- Leads are compliant, usable with PC board and ceramic substrates
- Minimum X-Y size, maximum board density
- Easy auto positioning
- Leads well-protected; being tucked under the board they are less subject to damage
- Easy replacement
- Socketing easy
- JEDEC standards exist
- Stand-off from the board allows easy cleaning
- Largest line of available packages: from 18 to 68 leads. Higher pin count under development
- Easy to socket

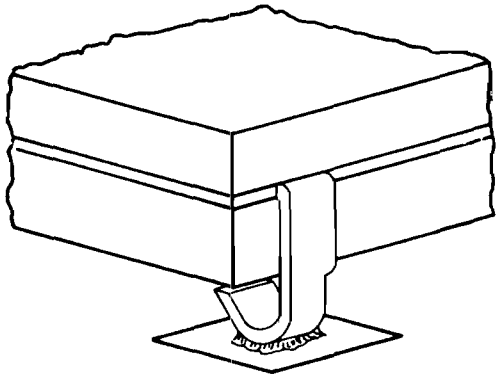
Disadvantages

- Total package height thicker than SOIC
- Infrared (IR) reflow difficult (difficult to solder)
- Invisible leads present testing, inspection and repair problems

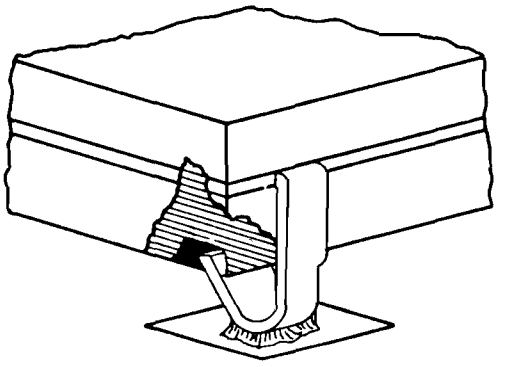
The popularity of the Gull Wing (or S-shape) packaging lead styles also have advantages and disadvantages which are listed below:

Advantages	Disadvantages
- Proven process Easy auto-positioning	- Leads are more susceptable to damage; exposed leads tend to bend and break
- Nested stacking (peripheral)	- Difficult to socket
- Allow for easy inspection testing, repair, replacement	- Real estate penalty

Figure 4c clearly illustrates the difference between compliant and non-compliant lead styles. Figure 4d shows the Gull-Wing/S-shape Lead Style.



Compliant J-Lead



Non-Compliant J-Lead

FIGURE 4c:
J-LEAD PACKAGE CONFIGURATION

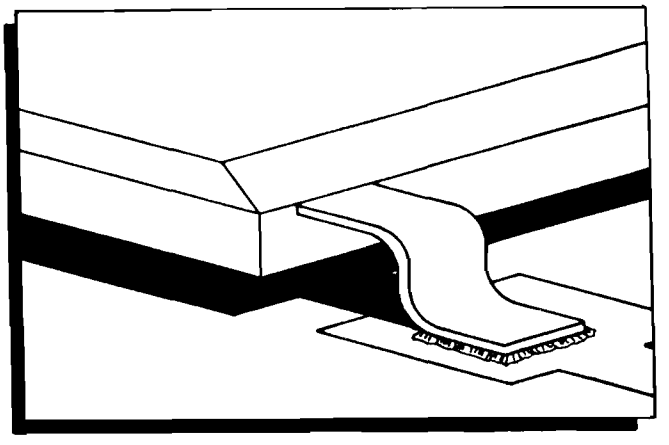


FIGURE 4d:
GULL WING OR S-SHAPE LEAD
PACKAGE CONFIGURATIONS

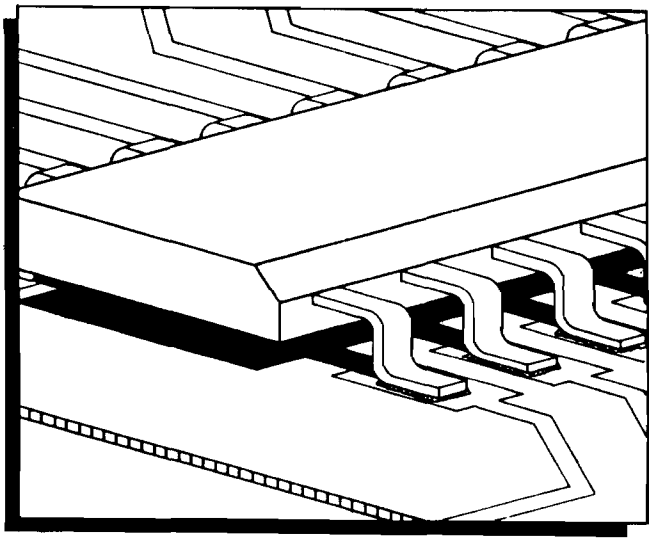


FIGURE 4e:
SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)
PACKAGE CONFIGURATIONS

Small Outline Integrated Circuit (SOIC) - Modified Dual-In-Line Package (DIP) with S-shaped (or Gull Wing) leads extending from two opposing sides of the package, capable of supporting the package off the mounting surface. The designation SOIC may have otherwise been derived from its origin as **Swiss Outline Integrated Circuit.** This package style generally houses small ICs of 28 I/Os or less. The package loses its attractiveness above the 28-pin count, at which point (1) the package becomes fragile and hard to handle, (2) lead-inductance problems begin to match those of the DIP and (3) board real estate advantages become insignificant. See Figure 4e.

Flat Package (Flatpack) - Square package with peripheral ribbon-type leads (3 to 6 mils in thickness) on two or all sides of the package. These leads are not designed to support the package but to act as a flexible interconnect between the package and the circuit board. This package style is one of the oldest forms of chip carriers as it emerged as an alternative to DIPs. The package was not widely accepted due to excessive lead length, lead resistance and the need for special handling procedures.

QUAD - This is a generic term for a chip carrier with leads on all four sides. **QUIPs** or **Quad-In-Line Packages** are similar to QUAD packages except that they are constructed with two staggered rows of pins along each longitudinal edge. The QUAD is an updated version of the original Flatpack with lead shapes often of the Gull Wing style.

Pin Grid Array (PGA) - Square package with axial-type leads extending from the bottom or top of the package that are used for through-hole mounting or, where leads are modified, for surface mounting **(LGA or Leadless Grid Array).** Configurations for these devices are generally intended for highly integrated devices consisting of 84 pins or more.

Sockets - Interconnection devices which are used as a link between the chip carrier and the PCB. This type of interface device may be utilized for a variety of reasons including:

- Sockets provide a low profile and low cost means of attachment while taking up little board area.

- Sockets are utilized for their ease of assembly, ease of replacement and inspection after assembly. They allow for rapid chip replacement in the field and spontaneous changes during equipment development phases.

- The sockets may also be used to house leadless devices which may not be readily available in leaded versions.

- Sockets provide protection to the chip from the thermal shock of soldering.

- Sockets promote the avoidance of board damage arising from the difficulty of removing ICs.

SECTION 3: IMPLEMENTING SURFACE MOUNT TECHNOLOGY

The establishment of reliable, low-cost manufacturing methods is integral to the successful production of surface mount assemblies. There are a number of primary considerations which need to be addressed prior to implementing SMT.

The processing steps for surface mount assembly are illustrated in Figure 5, and each step is delineated in the following text.

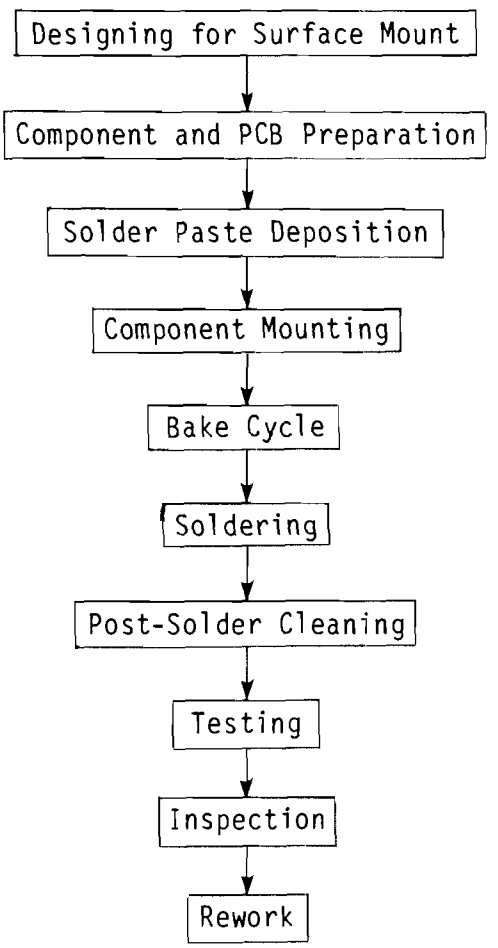


FIGURE 5:
SURFACE MOUNT ASSEMBLY PROCESS

Designing for Surface Mount

Designing surface mount assemblies requires that close associations must exist among all of the functions involved with producing an end product; that is, each facet of the processing cycle is an integral part of the finished product and the viability of each individual element is hinged on the success of the other. Therefore, at a project's inception, it is imperative that the designers be intimately involved with the processes of manufacturing, production, cleaning, inspection, test, rework, etc.

Practical design considerations include package size and shape, proximity between components, orientation of components and compatibility between component and printed circuit board. The package size, shape, orientation and proximity to other components determines the number of components per board or overall board size; the type of package also determines the accessibility to test, repair, replacement, etc. The PWB must be able to accommodate the components based on its ability to provide adequate routing or interconnection wiring.

The computer aids for design and manufacture now utilized for conventional mounting must be reassessed and enhanced to handle the inevitable changes that will occur in the transition from conventional designs to SMT. The use of double-sided boards will require interactive routing techniques and strategies to ensure accurate layouts. The compatibility between existing designs and component types as well as their reliability and availability will all have to be examined.

Table 5 lists the relative advantages and disadvantages of implementing surface mount components into the design and manufacturing environment. Table 6 compares the practical application considerations of leaded and leadless chip carriers.

TABLE 5:

THE ADVANTAGES AND DISADVANTAGES

OF SURFACE MOUNT COMPONENTS

Advantages	Disadvantages
• Small footprint on the circuit board enables higher circuit board density packaging. The chip carrier uses approximately 20% the surface area of its DIP equivalent and requires less than 33% of the substrate or PWB area.	• Need for circuit and manufacturing process redesign.
	• Large expenditures for new equipment and assembly techniques associated with conversion.
• Devices can be mounted on both sides of a circuit board, taking advantage of valuable circuit board real estate.	• Minimal package-style standardization; surface mount packages from different manufacturers often differ in lead finish materials, package dimensions, lead thicknesses, widths and spacings.
• Reductions in circuit board area yield shorter interconnecting printed circuit traces, increasing circuit performance.	• Inspection of solder joints underneath packages is difficult.
	• Testing and rework are more complicated.
• Smaller-volume packaging (smaller and lighter) is more rigid than standard DIPs which make it resistant to shock and vibration.	• Thermal cycling, power cycling and heat dissipation are critical reliability issues.
• Switching times (propagation delay) are reduced and higher speeds of operation can be obtained as a direct result of minimizing lead length.	• Overall availability of active and passive components is limited.

TABLE 5:
ADVANTAGES AND DISADVANTAGES
OF SURFACE MOUNT COMPONENTS (CONT'D)

Advantages	Disadvantages
• Shorter internal metallized conductors to the external pins means less pin-to-pin capacitance, resistance and inductance. In fact, trace inductance and line-to-line capacitance are approximately an order of magnitude less than their DIP equivalents.	• Currently a premium price is paid for components.
• They provide the same degree of reliability as the equivalent DIP.	
• Numerous active and passive components are available in leadless and leaded chip carriers.	
• Surface mount components and PWB footprints can be automatically pretested 100% and burned-in prior to assembly.	
• Shipping and handling costs are reduced.	
• The long-term projected SMC cost is half that of DIP equivalents and reduces to one quarter for large IOs (i.e., 64 pins or greater).	

TABLE 6:
CHIP CARRIER APPLICATION CONSIDERATIONS

Consideration	Leadless CCs	Leaded CCs
Thermal expansion match to PWB	Critical (noncompliant lead)	Less critical (compliant lead; provides flexibility)
Removal and replacement	Comparatively easy with special tools, damage to components or substrate is minimal	Less risk of damaging PWB metallizations but greater risk of damaging leads
Solder joint inspection	Difficult due to minimal component stand-off height	Less difficult due to greater component stand-off height
Flux removal after soldering	Difficult	Less difficult
Socket compatible	Yes (except JEDEC Type C)	Yes (except JEDEC Type B)
Lead length	Minimal	Moderate (inductance greater)
Heat transfer	Good (direct heat conduction path to PWB)	Good (leads help to dissipate heat)
Preparation for soldering	Barrier material coating of terminations required for proper solderability	Barrier material coating of terminations required for proper solderability

TABLE 6:
CHIP CARRIER APPLICATION CONSIDERATIONS
(CONT'D)

Consideration	Leadless CCs	Leaded CCs
Self-centering	Usually	Less of a given
Flexure of PWB	Critical	Less critical
Testability	Difficult	Less difficult
Profile	Lowest	Good
Automatic Placement	Easiest	Loading and handling are more critical

Components and PCB Preparation

Pretinning of metallized surfaces is a process which is recommended because it enhances good solderability, which in turn produces a secure electrical and mechanical connection. The process allows for the inspection of all metallized surfaces prior to installation, increases solder strength, increases slightly the distance between the chip and the board to enhance the cleaning process and inhibits the formation of intermetallic compounds. The risk of contamination in the solder joint is a relatively important reliability factor and pretinning helps to alleviate these potentially detrimental compounds from forming.

Solder Paste Deposition

Solder pastes are a composite of solder alloy and flux. The alloy (containing metal particles) forms the electrical and mechanical connection between the component and the substrate. The flux keeps the metal particles evenly dispersed and suspended throughout the paste until such time that the soldering process takes place.

The application of solder paste (or cream) to a PWB provides a means of holding the components in place on the substrate until soldering occurs; the paste also acts as a flux to facilitate solder flow. Fluxes are used to break up and remove tarnish (caused by oxidation) on metal surfaces and to provide protection to the metal during the soldering process. It is important that the flux remove the oxidation and keep the surface clean until the solder application has commenced; however, the flux strength must be limited to removing only the surface tarnish, to resisting attack of the metal and to ceasing reactions after the soldering process is complete.

Precise application of solder paste is considered a critical step since the solder joint forms both the electrical and mechanical connection. The process can be administered in a number of ways including: screen printing, which is currently the most widely used

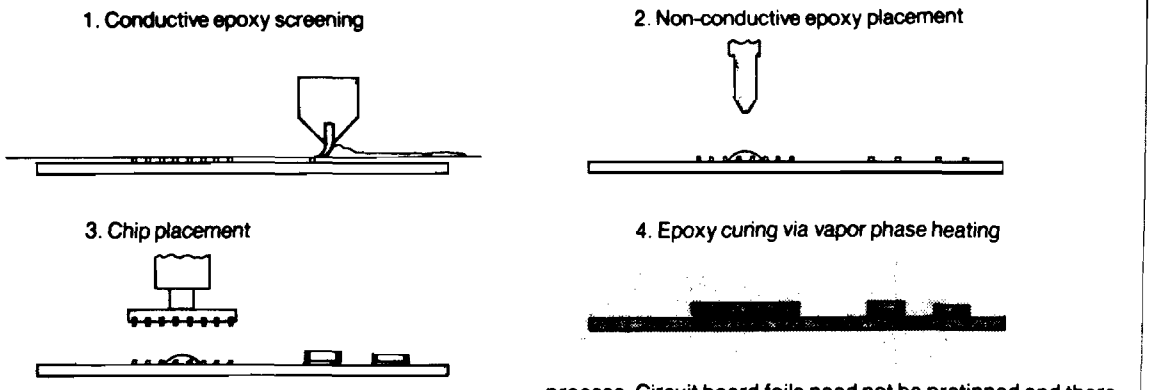
technique; application by stencil printing; and also by dispensing the material with the use of pneumatic equipment or by hand using a syringe. The solder placement should be inspected to determine if misalignment has occurred or if insufficient, excess or smeared solder is apparent. The vapor-phase soldering technique primarily employs solder paste in its processing scheme.

An alternative to solder paste is solder preforms. The preforms (usually spheres of solder) are positioned and held in place with a template or a tacky flux until soldering takes place. The Solder Transfer Application Technique (STAT) is another method whereby solder paste is screened onto a non-wettable surface in a pattern corresponding to the substrate land pattern. The components are then placed on the paste and the solder is melted. After cooling, the components are lifted off with uniform amounts of solder left on each of the pads.

The availability of numerous solder alloys for surface-mounting requires that the selection be made for each particular application dependent upon the expected operating conditions. Each alloy has distinct characteristics of melting point, mechanical and fatigue properties which necessitatesindividual evaluation.

Adhesives tack and hold components to the footprint of the PWB in preparation for another solder application technique called wave soldering. Sometimes adhesives are used in conjunction with solder paste when both methods, solder reflow (e.g., vapor phase) and wave soldering, are used. Adhesives come in both conductive and nonconductive forms. The nonconductive epoxies maintain their dielectric properties well over time and are more resistant to moisture than other adhesives. Epoxies cure rapidly with heat and provide strong, resilient bonds; they are available in different varieties and can be dispensed in a number of different ways. However, the cure times and temperatures of some epoxies may require conditions in excess of what a board/component can withstand without damage. The selection of a surface mount adhesive is dependent upon its thermal and electrical

conductivity characteristics. By comparison, the selection of silver adhesive as one of the most conductive materials is considerably less-conductive than typical solders (Ref. #10). See Figure 6, "Soldering with Epoxy."



Some surface-mounting attachment techniques use epoxy instead of solder. This method has been used for many years to produce hybrid circuits on ceramic substrates. But proposed surface-mount applications will use standard glass epoxy boards. Epoxy attachment may cost less than soldering processes in some surface-mount applications.

The process begins with the screening of electrically conductive epoxy onto the circuit board at the component attachment points. Drops of non-conductive epoxy hold larger components. Placement machines then position surface mount devices on the board. Convective or vapor phase heating then cures the epoxy. Curing time can occur in minutes and is temperature dependent.

The epoxy process has two key advantages. First, it consists of fewer manufacturing steps than the soldering process. Circuit board foils need not be pretinned and there is no need for a solder flux removal/cleaning step. Second, conductive epoxies can be formulated to minimize the effects of thermal expansion coefficient mismatch between chip and board materials.

The use of conductive epoxies has some drawbacks. The material is three times more expensive than solder. And "epoxy bridges", unlike solder paste bridges, will not clear themselves when heated. Mixed assemblies are not practical because epoxy must be applied manually to through-hole connections.

In some cases conductive epoxies may replace copper circuit board foils. Epoxy "foils" are merely screened on copperless boards, thus eliminating copper plating and etching. Though the process reduces manufacturing costs, the reliability of epoxy traces has yet to be determined.

FIGURE 6:
SOLDERING WITH EPOXY (REF. #11)

Component Mounting

Flexible mechanical assembly systems are required to accomodate the variation in PWB materials, component configuration, size and placement orientation inherent in surface mount assemblies. The placement of surface mount components is a procedure which is performed under close scrutiny. The tight tolerances of densely packed boards contructed with low-pitch packages indicates that placement accuracy is essential, even though some misalignment is acceptable due to the surface tension characteristic of molten solder which helps to align the components to

the PWB footprints. The placement process can be achieved by hand or by automation (pick-and-place equipment). Hand-placement becomes difficult due to the relative size of the components and corresponding footprints, especially in dense areas. The pick-and-place equipment runs into difficulty as requirements increase for handling numerous components with differing configurations, tolerances and dimensions.

Pick-and-place equipment selection is generally based on the user's requirements for speed and component variety. The equipment speed directly affects production volume, and, in fact, these equipments are rated by the number of components which can be placed per hour. The mechanical functioning of the system is classified into four basic categories, depending on the type of assembly and the variety of components. An essential requirement in SMT processing is that equipment be readily reset to handle a new product line with high placement accuracy and repeatability. The four basic equipment categories include:

(1) Inline Placement - This process requires that the substrate progresses past a fixed-position placement station where a single device is placed on the substrate.

(2) Sequential Placement - The component is selected from a feeder for placement on the substrate in this procedure. Either the placement apparatus (the head), the table holding the board or both move in the x and y directions to accommodate component placement.

(3) Simultaneous Placement - This process populates a section of a board or an entire board at one time by utilizing multiple heads to transfer an array of components to the substrate in a single step.

(4) Sequential/Simultaneous Placement - This system, containing a table capable of moving in the x and y directions, passes a board under multiple heads, each head placing a single component.

An important aspect of component mounting is the delivery of the devices. Theoretically, the bulk delivery of components used in automatic placement equipment is the optimum means of accomplishing this task. Components also arrive on reels of tape as a popular mechanism of delivery. However, the cost is an inhibitive factor as well as the complications of incoming inspection and test, since the devices must be removed from the tape. Cartridges and rails are both expensive techniques for use with automatic placement equipment but are readily available and widely used.

A whole new area of ESD-protective packaging concern deals with surface-mounted components. In the past some of these devices have been shipped in magazines just like DIPs and others have been shipped in bulk: but the preferred method of shipping SMCs today, for high volume production, is on reels of tape. The taping and reels may or may not conform to EIA Standard RS-481A, "Lead Taping of Surface-Mounted Components for Automatic Placement." This standard, however, does not address the subject of ESD protection.

For adequate ESD protection, when ESD-susceptible SMCs are shipped mounted on tape, both the carrier tape itself and the cover tape should be made of an antistatic material. The adhesive used to hold the devices to the tape must also be carefully selected such that it generates a minimum triboelectric charge as the devices are removed from the tape. Additional protecton may be afforded with the use of air ionization in the vicinity of component removal. "Faraday Cage" protection may be incorporated with the addition of an outer bag or container to ensure the safe transportation of the loaded reels (Ref. #12).

Bake Cycle

Baking populated substrates prior to soldering is performed to drive out any volatile material that would out-gas during the soldering process, causing the solder paste to splatter and solder balls to form.

This process evacuates air and flux pockets which may exist in the solder paste in an attempt to minimize potential volatility during soldering. The bake cycle is considered critical in the minimization of uncoalesced solder particles which may cause shorts or the release of solvent which may cause misalignment. Without regard to the actual solder paste composition, a bake cycle should be implemented after component placement and prior to soldering. The bakeout minimizes the effects of volatility in the soldering operation, enhances the self-alignment characteristics of the components and minimizes the generation of solder balls.

A preheat treatment for adhesive-attach assemblies has also been found to be a complimentary factor attributing to the success of SMC wave soldering. The preheat serves to remove harmful solvents from the flux and ensures better soldering.

Soldering

The significant role that soldering has played in the electronics industry is due to the relative ease and speed with which highly reliable electrical and mechanical joints can be made by automated mass-soldering machines at a low cost.

The process of soldering consists of joining two metal surfaces by melting a relatively low-temperature metallic material between the two. The IPC-S-804 specification "Solderability Test Method For Printed Wiring Boards" (Ref. #13) defines solderability as "the property of a metal to be wetted by solder." Wetting is thusly defined as "the formation of a relatively uniform, smooth, unbroken and adherent film of solder to a base metal." In order to ensure proper solder joint formation and strong surface bond strength, the wetting process requires that the metal surfaces be clean.

The specific choice of soldering technique employed is generally dependent upon the type of assembly being fabricated. There are three basic board assembly variations:

(1) Type I Assemblies are constructed with surface mount components exclusively. The components may be assembled on the top, bottom or both sides of the board.

(2) Type II Assemblies are a combination of both surface mount and through-hole components assembled on the top, bottom or both sides of the board.

(3) Type III Assemblies contain through-hole components attached to the primary (top) surface of the PWB and small surface mount components (generally discretes) affixed to the secondary (bottom) surface.

Soldering technologies are advancing in step with the rest of the industry by providing several processing techniques suitable for surface mount assemblies. Wave soldering, traditionally the soldering technique used to attach through-hole components, is being modified to handle surface mount components as well. Concurrently, other methods are being introduced to accommodate the growing number of surface mount assemblies.

Wave Soldering

Components are glued to the PWB surface with adhesives and then the assembly is moved through a wave of molten solder or dipped into a molten solder bath, immersing the component-side of the board. Both sides of the board can be soldered simultaneously if the angle and the speed of the process are properly controlled. DIP soldering of board assemblies is the process where the boards are lowered onto and floated on the surface of molten solder. Dragging a board assembly across the top of a molten solder bath is the other wave soldering approach. This process is designed to allow escaping gases to dissipate as the board undergoes soldering; however, the solder height and solder penetration into dense component lead areas is difficult to control.

Component, height, orientation, density and preheat temperature affect the wave's ability to converge after passing a component (see Figure 7). Therefore, the wave soldering process affects the formation of solder joints in the following ways:

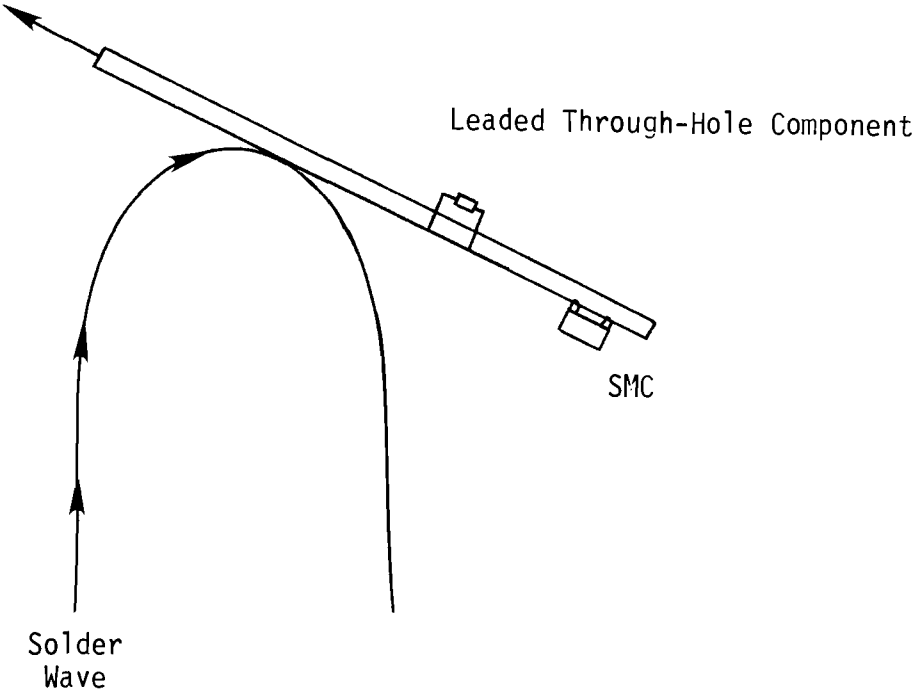


FIGURE 7:
WAVE SOLDERING OF A SURFACE MOUNT ASSEMBLY

- emergence angle of assembly from solder wave or bath
- board velocity
- heating capacity of the board, the component and the solder
- joint cooling rate

Vapor Phase

This soldering technique is referred to as reflow soldering. Reflow soldering requires that a solder paste be deposited along sites on a PWB where SMCs are to be placed. This paste holds the components in place until the assembly is soldered. The soldering process subjects the assembly to temperature conditions such that the paste melts, or reflows, to form solder joints.

The vapor phase processing technique is an extremely consistent soldering method whereby heat is transferred to the components and the board through an atmosphere of condensing vapor material. The soldering temperature is maintained constantly at the boiling point of the primary fluid so that the components are heated evenly and not subjected to localized overheating. The desired soldering temperature can be tailored for a specific application by changing the composition of the vapor phase.

The soldering process consists of moving a populated board into the vapor zone where a rapid uniform heating of the entire assembly occurs, regardless of geometry. This soldering method allows for the simultaneous reflow soldering of both leadless and leaded components. The board is moved into a secondary vapor zone for defluxing, cooling and drying. The finished boards emerge uniformly soldered, with minimal contamination, and the flux remains pliable, affording easy clean-up. See Figure 8.

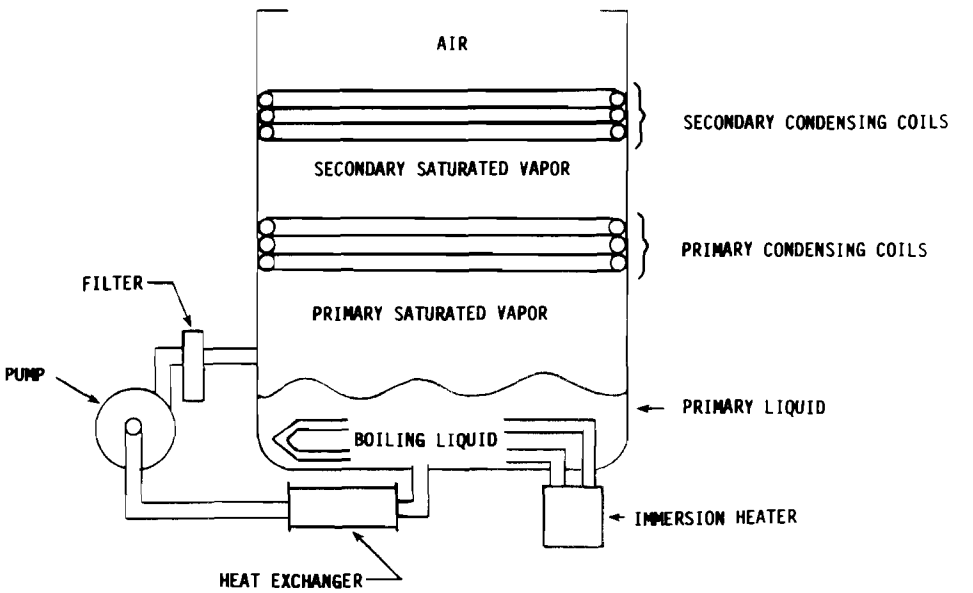


FIGURE 8:
VAPOR PHASE SOLDERING

Hot-Tip Method

In 1981, Texas Instruments developed a hot-tip method of attaching PLCCs to PW boards. This method utilizes a metal tip, which is electrically heated. The chip carrier is picked up and held in place by a vacuum. Solder flux is dispensed onto the chip carrier land area of the PW board. The hot tip/chip carrier combination is brought in contact with the prefluxed pretinned PWB. After the solder is reflowed by the hot tip, the PLCC is pushed into the flowed solder and held there for a short period of time until the solder solidifies and the tip can be removed.

Conduction - Reflow Belt Soldering

This soldering method conducts the heat necessary for accomplishing reflow of the solder between the component and the PWB by controlling the heat of platens. A series of platens (metal plates) is located beneath a continuously moving belt where the assembly is seated. The platen temperature and belt speed are individually controlled so that variations in reflow profiles can be achieved for different surface-mount assemblies. This hotplate technique is useful as a reflow system or for heating assemblies. The part temperature is raised rapidly to reflow temperature with little preheating. Curing of the solder cream prior to reflow on a hotplate is useful as a method of reducing spattering and/or solder balling.

Infrared

Infrared (IR) ovens are useful in the heating of a wide variety of assembly configurations; however, the system must be adjusted for each circuit design to accommodate the mix and arrangement of components. The assembly is placed on a belt and sent through a preheating zone, then spiked to reflow temperature to thoroughly heat the paste and then rapidly cooled to provide good solder adherence and uniform solder joints.

Infrared energy is transmitted in line-of-sight paths; therefore, large components may shield adjacent smaller components from exposure and consequently from proper soldering. Also, the different materials used in electronics absorb infrared energy at different rates. Solder creams readily absorb the energy due to the organics in the flux vehicle; however, the metal components within the paste reflect much of the heat which can cause localized overheating. Components sensitive to temperature should be shielded to prevent damage.

Post-Solder Cleaning

A post-solder cleaning performed immediately after soldering initiates the removal of flux residues which have not had time to congeal. This is a critical step in the process because remaining residues become a major source of circuit contamination. The residues are responsible for preventing the proper adherence of conformal coatings which can lead to corrosion. The long-term reliability of surface mount assemblies therefore rests on the prompt removal of this potentially hazardous material.

The cleaning process is almost exclusively carried out by various combinations of aqueous solutions (detergents or organic solvents) or by gaseous cleaning, which has also been found to be an effective cleaning process for surface mount assemblies.

Testing

Testing SMC assemblies has proven to be one of the most perplexing problems encountered by the users of this technology. The size and variety of components associated with SMT is often a deterrent to the functions of testing. Traditional bed-of-nails test fixtures are designed for 100-mil components, not the smaller-pitched packages of SMCs. The lack of extended solder pads on SMT assemblies restricts the use of test probes and consequently defies a relatively simple test solution.

New testing techniques are being developed to effectively assess these assemblies without minimizing their space-saving characteristics. Since surface mount assemblies are inherently difficult to test, new philosophies are emerging to accommodate this function. It is becoming increasingly apparent that testing schemes should be constructed as part of the system design process to determine the most desirable and feasible test points.

Increased board density requires that test probes, where they can be used, must be extremely small and yet sturdy enough to perform reliably under high-volume operation. The tight lead spacing neccessitates the use of specialized test probes which are designed to register readings without damaging the joint. Damage to a joint can occur when the force of the probe pressing down on the component is greater than what the solder joint can withstand. Therefore, unique designs in test probes are being implemented into new test equipment. At this point in time automatic test equipment is capable of testing PWBs containing surface mount components with 1.0mm lead spacings. Figure 9 is an example of test probes designed specifically to accommodate surface mount assembies.

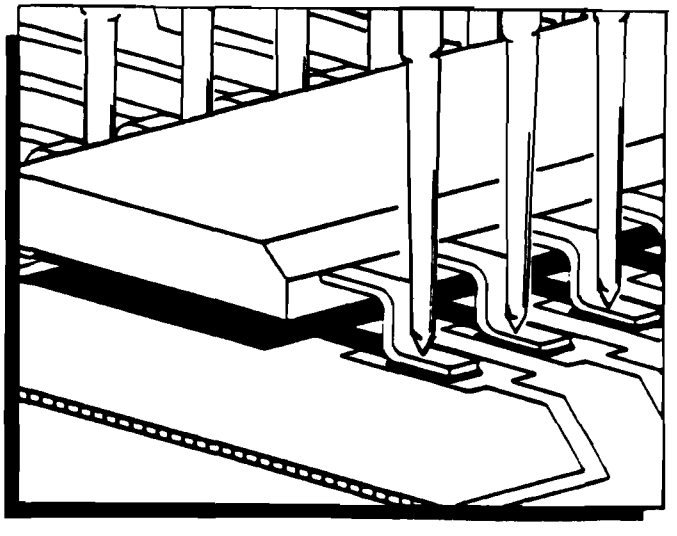


FIGURE 9:
TEST PROBES (REF. #14)

Qualification Test Requirements for Surface-Mounted Devices

The following criteria are representative of the test and evaluation standards for initial device qualification that the Rome Air Development Center (RADC) currently considers to be the baseline requirements for a reliable system (Ref. #15):

a. Temperature Cycling: -55 to +125 degrees Celsius (typically 1000 cycles) per MIL-STD-883, Method 1010.

b. Thermal Shock: -55 to +125 degrees Celsius (typically 15 cycles) per MIL-STD-883, Method 1011.

c. Moisture Resistance: temperature cycle over 25 degrees Celsius to 65 degrees Celsius in 90 to 100% relative humidity (typically 10 cycles) per MIL-STD-883, Method 1004.

d. Mechanical Shock: minimum 1500g level (or as dictated by system requirements when greater) per MIL-STD-883, Method 2002.

e. Vibration: 60Hz; 4 hours; x,y, and z planes with a peak acceleration of 20g per MIL-STD-883, Method 2005.

f. Constant Acceleration: 5000g level minimum per MIL-STD-883, Method 2001.

g. Salt Atmosphere: 24 hours at 35 degrees Celsius in a fog yielding a deposition rate between 10000 and 50000mg/sq meter per MIL-STD-883, Method 1009.

h. Power Cycle: operate device at full rated power while holding substrate at ambient temperature (number of cycles based on system power up/down projection).

i. Thermal Impedence θ_{JC} Testing (an effective thermal impedance test has yet to be determined).

The above tests are not intended to be an all-inclusive list but rather an example of the types of requirements that RADC feels are the minimum conditions under which surface-mounted devices need to be tested. These test conditions, excluding the thermal shock and mechanical shock (b and d) are also considered adequate device screening requirements.

Inspection

Inspecting the finished assembly goes hand-in-hand with testing to enhance the ability of identifying processing faults. This ensures the best degree of quality by allowing corrective actions to be properly implemented prior to the system entering the field. The initial evaluation of soldered assemblies can be accomplished by visual inspection for obvious faults. Solder defects can be identified as a misalignment of the surface mount component on the solder pads, the amount of solder coverage and texture, the presence of solder bridges or the size and uniformity of the fillet formation. X-ray and laser beam methods have been used with some success for the difficult task of solder joint inspection. However, solder joint inspection is more often based on manual methods, which have inherent problems such as detectability, repeatability, etc.

Preliminary tests, conducted as a minimum check, should identify the proper assembly of components by visual inspection for part orientation and unacceptable solder joints and electrical inspection for shorts or opens between adjacent signal paths. In-depth testing may be required at the completion of assembly including: burn-in tests to screen out defective devices; mechanical tests to determine the shear, tensile, flexural and torque characteristics of solder joints; and environmental tests to assess performance under conditions of possible exposure.

Rework

The rework of a printed circuit board includes the touch-up of solder joints that have been found unacceptable. The repair work is generally done by hand, and care should be taken to prevent subsequent damage to the substrate pads, the package and surrounding components during these repair actions. Each hand-solder application consists of a potentially dangerous thermal stress condition.

Rework depends upon the following:

- initial soldering technique
- type of solder
- temperature needed to reflow the solder
- thickness of metallization

The removal of a surface mount component can be accomplished in a number of ways. One method includes immersing those boards needing rework in a bath of molten solder oil hot enough to melt the solder. The component(s) needing rework are then lifted from the board. Another removal method requires the use of the soldering iron with a specially shaped tip to heat the contacts which will allow the removal of the defective device. A third approach utilizes a heat gun which heats up the SMC and surrounding area. Hot air is directed above and below the defective component creating sufficient heat to make the solder joints molten, facilitating quick removal. This approach is usually considered the most convenient and practical for rework.

The repair and replacement functions should be accounted for in the initial design by providing adequate space and compliance between components so as to minimize the expansion stresses. Also, to avoid overheating of other areas when performing rework, heat should be applied only to the area needing rework. Avoidance of indiscriminate heating will reduce the possibility of damaging adjacent components or PWB materials.

The solder joint rework required for the following surface mount assembly programs has historically proven that a high degree of quality can be achieved using this technology. Table 7 presents the results of the solder joint rework required for four Tracor Industry programs (Ref. #16).

TABLE 7:
A THREE-YEAR HISTORY OF
SOLDER JOINT REWORK

Program	Qty. Solder Joints	Qty. Rework	% Rework
JPL-Galileo (LCC Devices)	209,088	314	.15
GPS/Navstar			
LCCs	200,800	341	.17
Resistors	21,400	107	.50
Capacitors	2,600	26	1.0
F-20 CPU			
LCCs	40,256	61	.15
Resistors	3,959	30	.75
Capacitors	1,480	21	1.4
Miscellaneous			
SOTS*	7,200	0	0
Resistors	1,600	10	.62
Capacitors	1,400	28	2.0
Cumulative	489,783	938	.19

*Small-Out-Line Transistors

SECTION 4: LIFE CYCLE COSTS

Even though the history of the microcircuit industry has been relatively brief, its dynamic nature has chronicled tremendous technological advancement. The proliferation of concentrated, highly integrated circuit functions characterize the current trend in electronic equipment design. This developmental status has concurrently fostered a response to adequately accommodate these increased utilities with new design concepts, packaging strategies and manufacturing philosophies, each with implicit cost effects.

Established systems for fabricating traditional through-hole assemblies differ substantially from those required for surface mount processing, and, therefore, each step from system simulation through system design, testing and troubleshooting requires serious reevaluation for the applicability to SMT. This section explores the implications of SMT regarding system life cycle costs.

It is generally recognized that the total effectiveness of SMT is facilitated by automated manufacturing. The small component size makes labor-intensive hand-assembly impractical, and the accuracy attributable to automatic component placement evokes improved productivity, higher yields, consistent product quality, increased reliability and reduced costs. However, implementing an automated facility is an expensive capital investment.

To become a fully automated facility is a complicated and costly undertaking, one that requires an extensive and long-term commitment of time, money and planning. What is needed for successful implementation is a well-funded and coordinated plan with a dedicated team of managers, design engineers and production workers. According to Lewis Shioleno in Technology Takeoff Adds to Allure of Surface-Mounting (Ref. #4), this kind of project cannot be nickel-and-dimed to success; it will not work. The team approach and the total commitment of management makes the automated factory a success.

The economics of equipment expenditures is a major obstacle to many manufacturers interested in converting to SMT. DIP packaging and plated through-hole assemblies could exist on hand-assembly operations until volumes were such that automatic insertion equipment could be justified. That option is virtually nonexistent with SMT. However, when comparing the equipment needed for autosequencing, sorting, drilling, inserting and wave soldering required for leaded component assemblies, the process is less capital-investment-sensitive than might be first expected.

A pre-requisite for incorporating a highly automated process such as that needed for surface mount assembly production requires that it be cost-justifiable. Therefore, the cost of assembly by hand or by semi-automated means must be evaluated to determine the relative differences in total assembly cost, time, rework and waste.

The cost of hand-assembly may be half that of semi-automatic assembly or three-fourths as much as fully automatic assembly, but the cost in terms of product quality and volume must also be considered. Hand-assembly operations are potentially less reliable due to the direct human interaction and certainly incapable of the high-volume available with automatic assembly processes. The total life cycle cost from the initial outlays for redesign, assembly, cleaning, test, repair, replacement and spares straight through to obsolescence needs to be carefully studied.

Since automation's impact has such far-reaching effects, the alternatives which seem to generate the most cost-effective solutions will have to be justifiably apparent to the overall application. Product aspects affected by implementing an automated assembly process for SMT include:

- Facility Planning
- Material Handling
- Design
- Process Control
- Inspection
- Test
- Repair
- Reliability/Maintainability

The concepts motivating the invitation to develop and use SMT is based on sound business judgement and solid financial reasoning. The following delineate these justifications, which incidentally are based on the Japanese rationale of the 1970s (Ref. #17):

- Smaller electronic circuits consume less material and should, therefore, be more cost-effective. Circuits incorporating surface-mounted devices are designed to have components mounted on both sides of the printed circuit board. In some cases, this will allow up to a 50% reduction in circuit board usage. Each circuit, of course, must be analyzed on an individual basis. While some circuits will not yield the same space savings, future circuits incorporating surface-mountable IC chip carriers may provide even more than a 50% size reduction. Reduced circuit board size also reduces the use of conductor materials, solders, and solvents and increases the utilization of space required for such associated processes as curing/drying cycles.

- Placement equipment for surface-mounted componentry is more compact than equipment presently used for automatic insertion. This will allow for better utilization of factory floor space. It is important to consider future production requirements and the potential for meeting these requirements with existing factory space.

- Handling and storage of component inventory is a factor that is often overlooked when costs are analyzed. Many components are bulky and difficult to transport. In comparison, SMT components are more compact. This should help to eliminate problems encountered by companies that have moved their operations to offshore facilities and are now faced with long inventory pipelines both in shipping components to their factory as well as bringing finished products back to the U.S.

- Placement equipment for surface-mounted components will continue to improve as user experience increases. Machinery will be available for efficiently placing components at speeds varying from several thousand per hour to in excess of 100,000 components per hour, significantly boosting product volumes.

- Component manufacturers recognize that it will be difficult to expect a significant price premium for surface-mounted devices. The key to cost reduction lies with increasing production outputs. If we return to the principle that smaller components require less material, then the key to reducing costs rests with automation and improved manufacturing yields.

The evaluation of system costs at various intervals or stages of development can be a valuable tool in determining the overall life cycle costs. Equipment installation costs (in ballpark figures) resemble those found in Table 8 (Ref. #18). These costs are based on 1985 dollar values.

TABLE 8:
EQUIPMENT INSTALLATIONS (BALLPARK COSTS)

Dedicated equipment to provide essential functions of:

- Solder deposition
- Component placement
- Soldering
- Cleaning
- Inspection
- Test
- Repair

Installation examples:

Stage	Volume (Components/hr.)	Max Board Size	Ballpark Cost Range ($)
Experimental	60 - 100	4 x 4	3.5K
Laboratory	100 - 1000	8 x 8	23K - 43K
Pilot Line	1000 - 3000	12 x 14	105K - 350K
Production Line	5000 - 15000	14 x 18	295K - 745K

The research and development phase should evaluate the feasibility of the project and define the impact of the automation process in terms of cost for redesign and equipment investment strategies. An initial analysis should determine if SMT will directly enhance product quality or increase the product's competitive value in the marketplace. Contrasts need to be developed to determine the potential of the work content by manual, semi-automatic or fully automatic assembly means. Major operating-cost profiles need to be established to verify the significance of the move to SMT.

The laboratory stage and the pilot line stage should provide the answers to how much dedicated floor space will be utilized with this equipment, how to deal with mixing existing technologies with SMT and what kind of storage space/conditions will be necessary? Other questions which need to be addressed are: How much production volume will be required to meet the break-even point and how much tolerance will the system provide in terms of rework and waste? How much effort will have to be expended to retrain the work force? Factors which also pose big problems are how to deal with the availability, or lack thereof, of surface-mountable components and how to work around the uncertainties of current standardization policies. It is essential that these questions be answered prior to implementation.

The production line phase bears the biggest financial burden since the investment of time, labor and material all are gambled on the finished product. The total life cycle costs reflect the capital investment or acquisition costs, the volume of finished product available for sale, the quality of the product (i.e., yield failures, field failures and rework, all of which increase the production costs) and the cost of inventory.

A government source directly involved in monitoring the progress of setting up a typical functional SMT facility indicates that the capital investment required is upward of three million dollars with an

associated time commitment of approximately three years. The commitment is considered a minimum to become efficient in the utilization of the technology. Each manufacturing commitment will be based on requirements of volume and product type, which will influence individual investment. The ability to incorporate existing production equipment is attractive, but with the wide range of components to be handled and with fundamentally different design and manufacturing requirements imposed on each process the practicality is diminished.

Mounting pressure from both foreign and domestic markets demanding high-quality products has heightened financial as well as manufacturing efficiency goals. Since business profits from greater productivity and competition, today's competitive business environment necessitates that the appropriation of large capital expenditures be carefully scrutinized to determine the most profitable investment alternatives. However, the anticipated cost reductions associated with SMT may not be the only deciding factor; just as important is the competitive edge gained by the development of a smaller, lighter, more-reliable and functional product.

SECTION 5: SMT FAILURE MECHANISMS

The failure mechanisms introduced by surface mount technology have delivered new reliability concerns to the microcircuit industry. SMT directly and indirectly affects the failure mechanisms of the (1) package, (2) solder connection and (3) printed wiring board.

Rockwell International's success with SMT (Ref. #3) has been attributed to superior reliability. The failure rates of SMCs including ceramic leadless chip carriers have been found to be consistent with or lower than typical leaded components. There has been no indication of new failure trends resulting from this alternate packaging or assembly technique.

Surface mount technology has been touted as a highly reliable manufacturing technique since its inception. However, in retrospect there have been some serious problems encountered with its utilization, some of which have yet to be ironed out. First, it should be understood that the connections formed by conventional through-hole devices are relatively large and therefore more stress-resistant than SMC connections.

The stresses that DIPs encounter are effectively absorbed and distributed through the leads directly into the board. SMCs lose much of this advantage through decreased terminal dimensions, decreased stand-off height and, most importantly the strong mechanical junction formed at the board interface. The low stand-off height, mass and weight of SMCs do, however, contribute significantly to the reduction in device vibration levels.

New failure mechanisms have emerged with the direct soldering of leadless chip carriers to the surface of a printed circuit board. The difference in the thermal coefficients of expansion (TCE) between the

package and the substrate to which it is attached has been found to be a crucial reliability factor. Since the TCE of the package and the substrate typically do not match, they expand and contract at different rates during thermal cycling. The interface between the substrate and the package (the solder joint) has proven to be the weakest link in the assembly. The solder itself is the least-resistant material used in the process because it is exposed to the severest stresses. The solder joints also incur the most damage due to the concentration of stress induced by the cyclical loadings of power, temperature and mechanical vibration, most of which are a direct consequence of TCE differences.

To satisfy the strict reliability demands imposed on today's electronic products, surface mount technology has to overcome some of its current limitations. This investigation into the physics of failure for surface mount packages, solder joints and printed wiring boards will identify what has been discovered to be the prime reliability issues.

The information contained in the Reliability Analysis Center's dedicated reliability data base is given in Appendix A. The data presented in the tables of the appendix specifically supports the failure event criteria of chip carriers and flat packs. This failure event information is derived from failure analyses done at the component level which is divided here into two distinct groups:

(1) Failure Indicators
(2) Failure Locations

Failure Indicator data provides information on the first detectable effect of a part failure while the Failure Location data describes the physical location of a detected failure.

The data of Appendix A are summarized and presented as pie charts. Figures A-1 through A-16 describe graphically the failure mechanisms of both flatpacks and chip carriers.

Surface Mount Package Reliability

Devices manufactured for placement in surface mount packages are essentially the same as those placed in conventional packaging. The active elements are designed and fabricated with the same technology, reliability standards and manufacturing processes; therefore, the failure mechanisms are also similar.

Current circuit designs are denser and more complex, thereby requiring new ways to dissipate heat. Dissipating the heat of an operational component is a necessity due to the limiting effect that temperature has on the component's functional stability. Surface-mount components are not afforded the easy access to the internal board heat sink that DIPs are, whose leads penetrate the board surface. SMCs often rely on thermal vias to transport the heat away from the chip. Heat transfer by this mechanism is generally less efficient (by comparison) simply because the amount of transfer medium is reduced. Therefore, some of the excess heat is forced through the package itself into the surrounding ambient. This is particularly true of plastic packages. Since the lifetime of a device is directly related to the junction temperature, the concentration of thermal energy in these small areas poses a critical reliability issue.

Throughout an assembly localized high thermal concentration areas develop due to the unequal heating of components. The unequal heating is a result of mixing components on one printed circuit design which generate heat at different rates and to different degrees. The amount of heat generated is relative to the amount of power dissipated by each component and, therefore, a five watt device generates much more heat than a quarter watt device operated at the same rate. The unequal heating is realized in the differential expansion of materials which causes stresses to develop within the component packages and in the solder joints. Larger packages are subject to greater stress since the thermal conductivity is lessened by the increased amount of material through which the heat has to pass.

Solder Joint Reliability

Solder joints of surface mount assemblies function as both electrical and physical or mechanical connections and therefore constitute a major concern to the reliability of surface mount designs.

The poor solderability of printed wiring boards is estimated to cause 50% of the solder defects and approximately 20% are caused by the component lead solderability problems. The other 30% are possibly due to solder composition or processing methods but more likely due to the application of operating stresses.

Improper or defective solder joints may occur in response to a large variety of factors, including:

- Mechanical Considerations
  - Solder Joint Fatigue
  - Solder Joint Formation Anomalous Effects

- Metallurgical Considerations
  - Solder Composition
  - Wettability of Metallizations
  - Solder Contamination

- Chemical Considerations
  - Oxide Formation Effects
  - Cleaning of Flux Residues

Solder Joint Fatigue

A prime reliability issue associated with SMT assemblies involves the solder joint integrity between the surface-mounted component and the printed wiring board. Two typical forces which affect solder joints include:

(1) The difference in thermal coefficients of expansion (TCE) between the PWB and the chip carrier.

(2) The temperature differential produced between the two during powered operation.

Thermal stress results when materials with different TCEs are joined and exposed to variations in temperature. When the materials respond to thermal fluctuations, each at their own rate, the bond which ties them together (the solder joint) restricts their independent movement. The resulting damage to the solder joint is cumulative in nature; that is, as the number of temperature fluctuations increases, the solder joint progressively weakens and the probability of failure increases.

A worst-case scenario for solder joint fatigue is represented by power cycling with large temperature variations. The substantial changes in temperature coupled with materials which have widely differing thermal coefficients of expansion produce an extreme fatigue environment.

Figure 10 describes the stresses that develop in a typical surface mount assembly containing a ceramic leadless chip carrier and an epoxy-glass substrate.

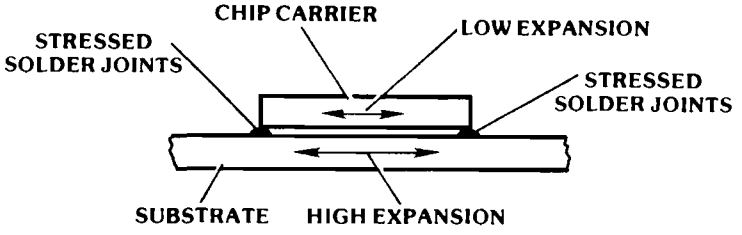


FIGURE 10:
STRESS CONTOURS OF A SURFACE-MOUNT ASSEMBLY

When stress is applied to the assembly, both the substrate and the component deviate from their original shape concurrent with their individual rates of expansion or contraction. This change will occur within the x,y or z planes, and the stress that results is directed to the solder joint within the plane of the circuit board.

The first applications of this technology utilized ceramic leadless chip carriers mounted on traditional polymer substrates. It was not long before solder joint cracking was being induced by the thermal loading imposed on the assembly. This situation was of course unacceptable and a remedy was sought to alleviate some of the burden felt by the solder joints. An obvious solution seemed to be the introduction of ceramic board substrates into the assembly as a mate for the ceramic chip carriers. The TCEs of the two materials would be identical, and, therefore, the stress levels in the solder joint would be minimized.

This remedy failed to produce the desired effect because it was discovered that not only does thermal cycling create stress in the solder but so does power cycling. Dissipating power at the component level has the potential to generate hot spots throughout the assembly, where the components heat up at a faster rate than the substrate, causing additional stress in the joint. Therefore, since the ceramic of the component package becomes hotter than the ceramic of the substrate the problem was not solved.

The philosophy of matching the expansion characteristics of various materials did not fully address the problem, and a new approach was considered. Engelmaier (Ref. #21) believed that a tailoring rather than matching of the coefficients is required when thousands of on-off power cycles are utilized in system functions.

Figure 11a establishes the assumed thermal expansion congruencies which would be achieved by mounting a ceramic chip carrier on a ceramic substrate. Figure 11b illustrates the variability of material thermal expansion properties.

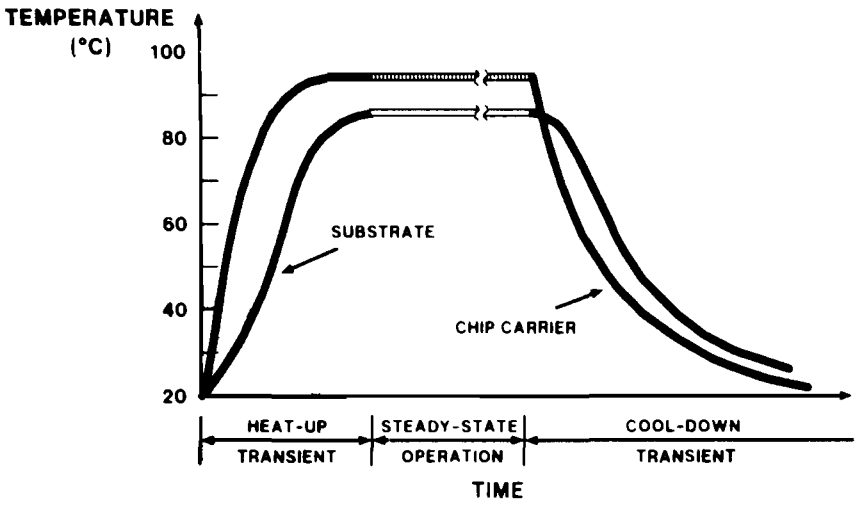


FIGURE 11a:

ASSUMED CYCLIC TEMPERATURE HISTORIES FOR CHIP CARRIER AND SUBSTRATE DURING FUNCTIONAL OPERATION

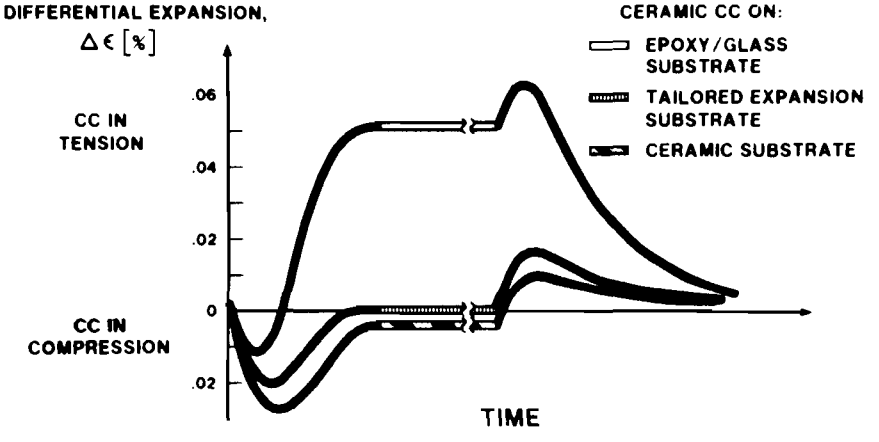


FIGURE 11b:

ILLUSTRATIONS OF THE VARIABILITY OF MATERIAL EXPANSION PROPERTIES

Table 9 establishes the TCEs of materials typically used in surface mount assemblies.

TABLE 9:
THERMAL COEFFICIENTS OF EXPANSION OF
VARIOUS MATERIALS

Material	TCE (XY) ppm/^{o}C
Plastic Composition Chip Carriers	6 to 7
$Al_2 O_3$ Ceramic Chip Carriers	5 to 7
Alloy 42	5
Copper-Clad Invar	5
Copper-Clad Molybdenum	5
Carbon-Fiber/Epoxy Composite	-0.5 to +2
Kevlar Fiber	-2 to -4
Quartz Fiber	0.54
Glass Fiber	4 to 5
Epoxy/Glass Laminate	12 to 16
Polyimide/Glass Laminate	11 to 14
Polyimide/Kevlar Laminate	3 to 7
Polyimide/Quartz Laminate	6 to 9
Epoxy/Kevlar Laminate	6 to 7

Solder cracking becomes significantly worse as the number of solder joints increases with package size and the power dissipation increases with die size and function. As a leadless chip carrier increases in size from 18 pins to 64 pins, the allowable TCE difference between the circuit substrate and the chip carrier must decrease from the typical 7 ppm/^{o}C to 2 ppm/^{o}C in order to achieve the same solder joint thermal cycles to failure. To achieve a TCE match of this magnitude, new circuit substrate materials must be used.

Test results confirm that conventional circuit boards (glass/epoxy and glass/polyimide) containing large ceramic leadless chip carriers cannot attain failure free operation for 500 thermal stress cycles (Ref. #23,#24). Figures 12a and 12b present the cumulative failure results of the testing.

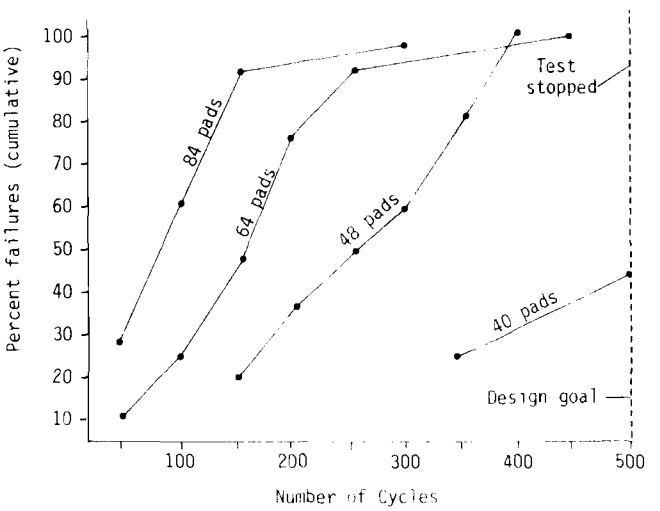


FIGURE 12a:
FAILURE RATE RESULTS FOR
EPOXY/GLASS BOARDS

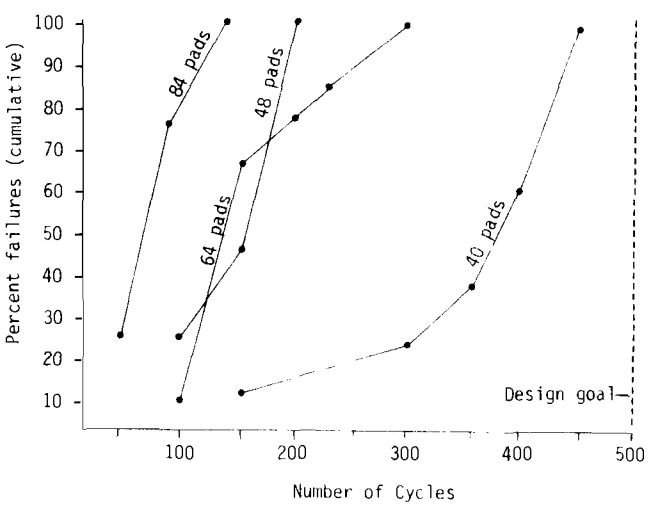
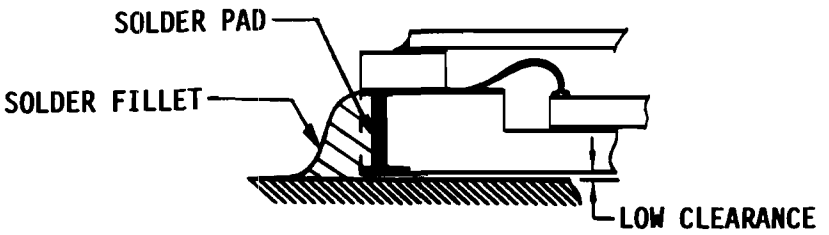


FIGURE 12b:
FAILURE RATE RESULTS FOR
GLASS/POLYIMIDE BOARDS

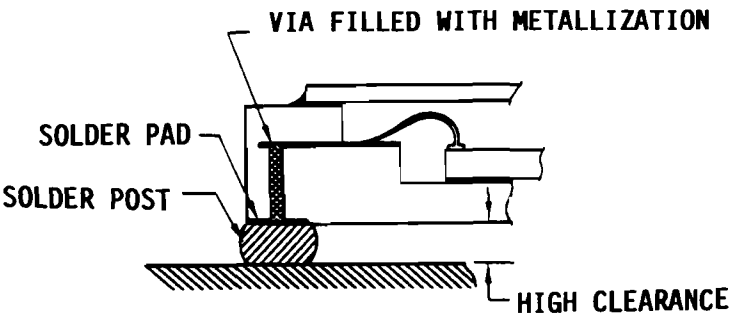
Solder Joint Formation Anomalous Effects

The formation of the solder joint is also an important factor in the reliability of the assembly. Investigations continue to determine the optimum solder joint configuration. The alignment, location, the degree of parallelism between the package and the substrate as well as the amount and shape of solder contained at each joint location all have a dramatic effect on how the solder joint reacts to stress.

Leadless chip carriers typically have metallized grooves (castellations) on their outer edges to connect the solder pads (which interface the package to the substrate) with the wire bonds (which interface the package to the die). Illustrations of two solder joint formations typically used with leadless chip carriers are given below in Figure 13a, a solder fillet, and Figure 13b, a solder post.



a. With Castellations



b. With Blind Vias

FIGURES 13a and 13b:
LEADLESS CHIP CARRIER SOLDER JOINT FORMATIONS

Solder Composition

The solder alloys themselves have fatigue properties which are inherently characteristic of the alloy composition. Their behavior, therefore, is largely dependent upon how that composition reacts to the thermal-mechanical stresses to which it is exposed. Solder alloy selection is based on its strength characteristic and its metallurgical compatability with the base metal with which it will form the bond. Over 90% of the solder used in the electronics industry is of a tin-lead composition (Ref. #25).

The tin-lead solders typically used in the soldering of surface mount assemblies are considered to be soft solders due to their physical behavior under stress conditions. Soft solders react to the mechanical tension by absorbing some of the stress; however, some deformation occurs with each stress load. After repeated load applications, the solder becomes permanently deformed which allows cracks to develop and propagate into failures.

Table 10 provides a list of various solder alloys along with their melting range, tensile strength and shear strength. Accompanying these statistics are application descriptions pertinent to the major composition categories.

The shape of the solder joint, the degree of solder coverage on the metallized footprint of the substrate and the solder height have all been implicated as potential solder formation concerns. It has been concluded that long-term reliability can be expected from 1.1mg of solder per connection, as an optimum condition, although solder amounts in a range of 0.6 to 2mg are acceptable (Ref. #26). Caswell states that consistent coverage of both the package and substrate can be accomplished with an 8.5 mil solder deposition on 20 x 25 mil footprints (Ref. #16).

TABLE 10:

SOLDER ALLOY DATA CHARACTERISTICS

(REF. #33)

Alloy	Melting Range (deg. C)	Tensile Strength (lbf/in^2)		Shear Strength (psi)		
		20 C	100 C	-130 C	25 C	150 C
62Sn/36Pb/2Ag	179					
63Sn/37Pb	183	6120	2700	12700	4130	1165
60In/40Pb	174-185					
60Sn/40Pb	183-188	2700	580			
50In/50Pb	180-209					
50Pn/50Sn	183-212			11100	3515	1100
96.5Sn/3.5Ag	221	5260		16600	4650	1510
95Sn/5Pb	183-222					
99Sn/1Sb	235			15100	2900	1125
95Sn/5Ag	221-240					
95Sn/5Sb	232-240	4410	2900	18150	4625	1880
80Au/20Sn	280					
10Sn/90Pb	275-302	2850	1160	7300	2800	1500
97.5Pb/2.5Ag	303			5300	2590	1440
97.5Pb/1.5Ag/1Sn	309	4980		5900	3040	1520
90.Pb/5In/5Ag	290-310			6220	3470	1755
95Pb/5Sn	310-314					
88Au/12Ge	356					

Remarks	
Sn/PB/Ag:	Ag prevents dissolution Ag from Ag or Ag or Ag/Pb conductor pads/terminations. It also increases strength. 5/93.5/1.5 or 1/97.5/1/5 are used in sequential soldering processes.
Sn/Pb:	Most widely used; high-lead alloy good for high-temp. soldering; may get excessive Au, Ag, and Cu dissolution.
Sn/Ag:	Thermal-fatigue-resistant, superior wetting, greater strength and creep resistance. 96.5/3.5 most common.
Pb/In:	Decreased crack propagation during thermal cycling as compared with 63Sn/37Pb. Excellent wetting of Au, Pd, Pt and much lower leaching of Au.
Other:	Au/Sn, Au/Ge, and Au/Si (experimental) for die attach and sealing.

Cases of insufficient solder amounts characteristically have cohesive solder failure as a typical failure mode. Cohesive solder failure is a failure where the lead has pulled out of the solder with solder remaining on both the lead and the substrate. Insufficient solder placement is often the cause of inadequately formed solder joints, whereby open connections and voids result. Excessive solder in a solder joint is responsible for solder bridges that develop between adjacent leads. This solder bridging creates a conduction path between leads which should be isolated from one another.

Increasing the clearance or stand-off height between the component and the board allows the strain which develops during cycling to be absorbed by the main body of the solder connection. A small stand-off height limits the area through which the strain can be absorbed which results in solder joint cracking. Figures 14a and 14b show the effects of solder height on interconnection reliability.

Solder joint strength is evaluated by torque or shear strength tests. Figure 15 relates the twist strength of 24-pin leadless chip carriers residing in a 150°C atmosphere to various stand-off heights. A logical assumption that might arise from testing devices in this manner is that the corner solder joints would fail first and therefore no longer contribute to the overall strength of the unit. According to Ref. #27, "the torque to failure is the cumulative sum of the torques for the individual joints. If some pads are intentionally left free of solder, the twist strength is practically proportional to the number of solder posts remaining."

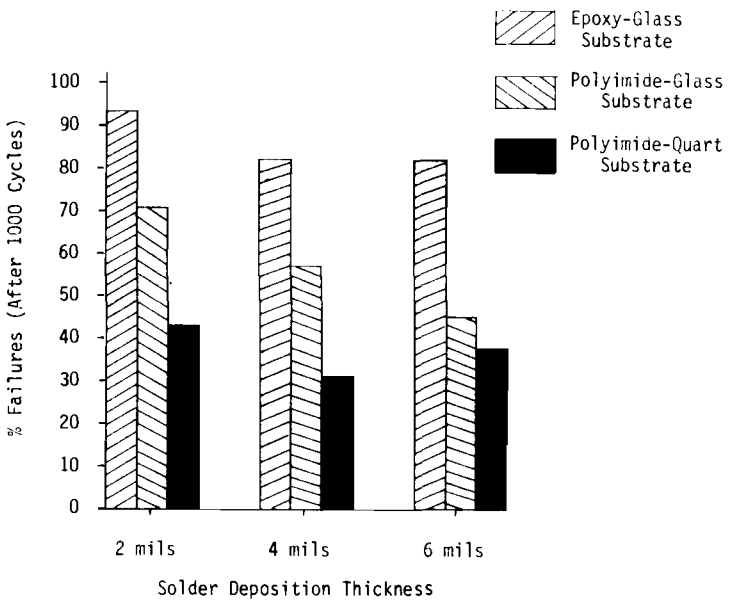


FIGURE 14a:
SOLDER HEIGHT VS. INTERCONNECTION
RELIABILITY (REF. #28)

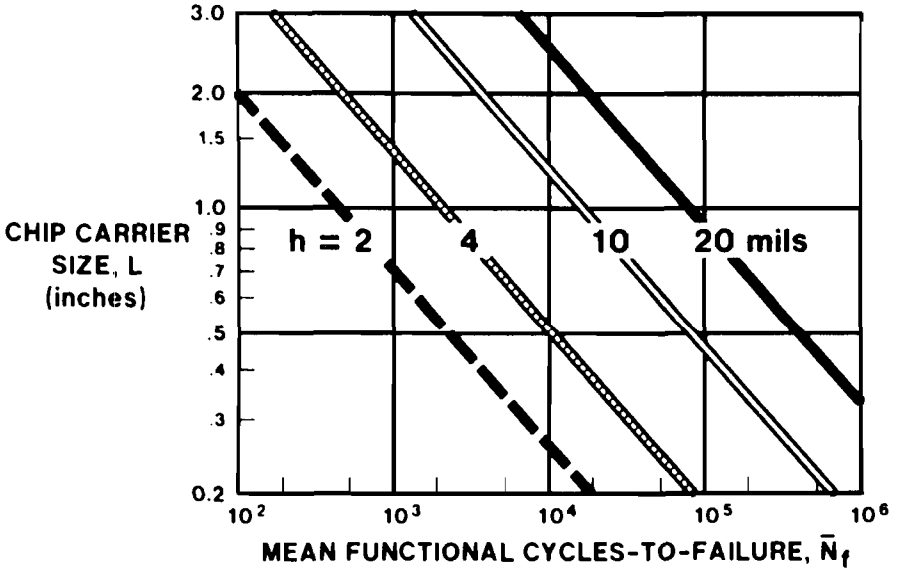


FIGURE 14b:
THE RELIABILITY EFFECTS OF CHIP CARRIER
SIZE AND SOLDER JOINT HEIGHT (REF. #29)

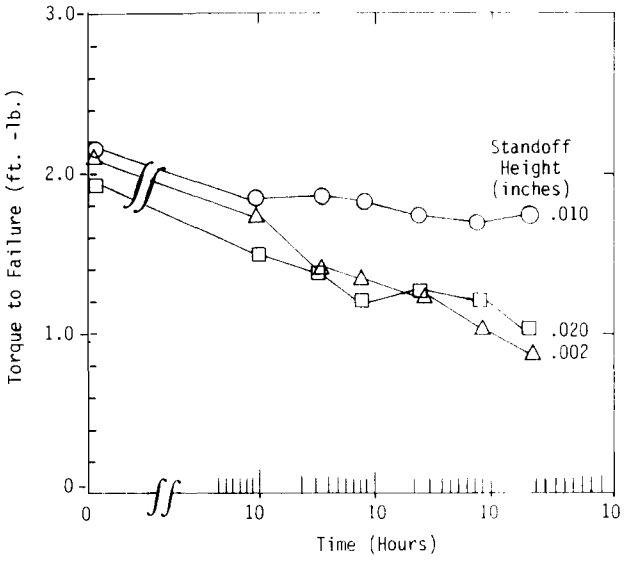


FIGURE 15:
TORQUE STRENGTH VS. STAND-OFF HEIGHT
(REF. #27)

Wettability of Metallizations

The formation of a good solder bond is based on a compromise in that the surface materials must dissolve partially in the molten solder in order to provide good wetting but not so much as to initiate intermetallic compound growth. The solder flux ideally acts to provide the required wetting between the surfaces being attached in typical solder connection processing. Poor solder joint formations can be the result of dewetting or inadequate surface preparation. This condition, also referred to as cold soldering, indicates that a lack of proper adhesion has occurred between solder surfaces. Cold solder connections often can be detected by visual inspection.

Solder Contamination

Surface mount terminations are generally formed from or coated with precious metals such as gold, silver, platinum, palladium, etc. These terminations are readily soluble in solder, and if left unprotected the terminations become contaminated when placed in contact with solder. The intermetallic compound formations which result from the interaction between the active solder components (tin) and the soluble metallizations (precious metals) produce weak solder joints at elevated temperatures. The process of intermetallic compound formation can be controlled by proper heat treatment, choice of solder alloy or the use of an underlying film (nickel) as a barrier to inhibit the dissolution of materials. The use of barrier materials has been widely accepted as a means of providing an interface between the termination and the solder, thereby protecting each from contamination. Figure 16 is an example of how barrier materials are used.

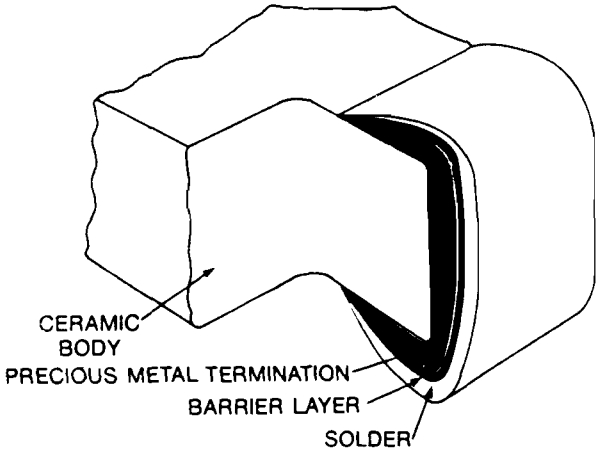


FIGURE 16:
TYPICAL COMPONENT TERMINATION SHOWING BARRIER LAYER TO PREVENT PRECIOUS METAL INTERMETALLIC COMPOUND FORMATION WITH THE SOLDER

The intermetallic compound formations produced by the dissolution of component lead material into the solder is responsible for the contamination of the solder joint. Any precious metal which dissolves into the joint becomes a problem which is aggravated as the concentration of the metal increases. This typically is expressed as a solder joint which becomes consumed by the process of diffusion between the precious metal and the tin in the solder. This consumption process is initiated as the molten solder comes into contact with the surfaces to be joined but may also continue throughout the life of the joint.

This contamination process is responsible for producing rough or gritty surfaces which reduce the ductility of the solder joint. This loss in the plastic response behavior of typical solder can be influenced by a relatively small amount of contamination. The contamination reduces the yield point (i.e., the point on the stress-strain curve which separates elastic and inelastic deformation) and causes the solder connection to be sensitive to even smaller temperature fluctuations. See Figure 17a. A consequence of this condition is the effect on the fatigue life of the joint; see Figure 17b.

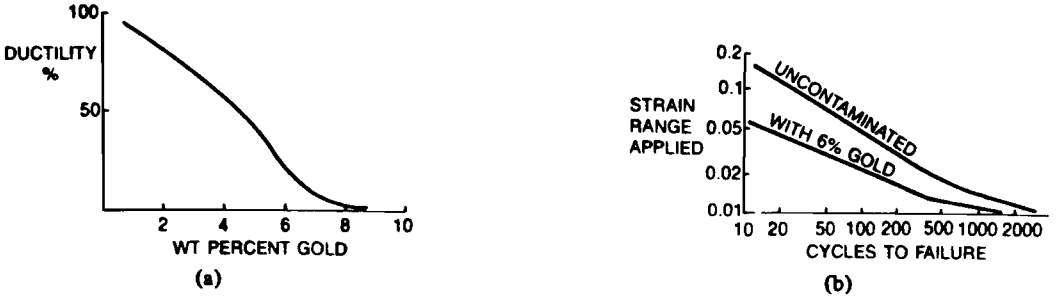


FIGURE 17:
HARMFUL EFFECTS OF GOLD IN EUTECTIC SnPb SOLDER.
17a: REDUCED DUCTILITY; 17b: REDUCED FATIGUE LIFE
(REF. #24)

This contamination is also responsible for the formation of brittle solder joints which fail characteristically at much lower temperature stress levels than would ordinarily be expected. As an example, a contaminated solder joint will fail when stressed at a few hundred thermal cycles in contrast to the thousands of thermal cycles of a contamination-protected joint.

The dissolution of these metals decreases the melting point of the solder itself, which makes assembly and rework difficult. See Figure 18.

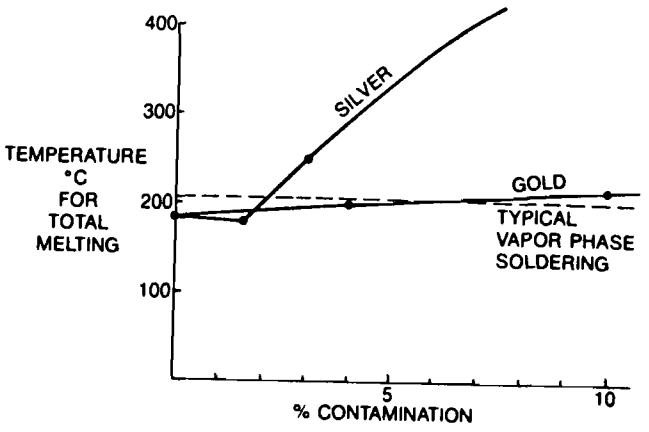


FIGURE 18:
INCREASE IN MELTING TEMPERATURE FROM PRECIOUS METAL CONTAMINATION (REF. #24)

Oxide Formation Effects

Surface-mounting relies on the component being supported during solder reflow by the surface tension forces of the solder. When molten solder is exposed to air it quickly forms an oxide skin which can reduce the surface tension of the solder by a factor of two. This skin formation is particularly detrimental to surface-mounting where surface tension plays a major part in successful soldering operations. Careful monitoring of the soldering process is required to ensure the application of quality solder. Reduced exposure to oxidizing agents and other contaminants is a must in the formation of reliable solder connections (Ref. #30).

Cleaning of Flux Residues

The criticality of removing flux residues prior to performing the soldering process is evidenced by the number of voids formed in the solder. Trapped air and flux forcefully escape from the solder, leaving behind harmful voids. Defects such as voids in a solder joint have a large effect on the fatigue resistance of a solder joint. Voids become stress-concentration sites which alter the typical stress patterns. It has been found that such defects can reduce the life of a joint up to as much as one-half (Ref. #25). Figure 19 compares solder joint failures of affected and non-affected joints.

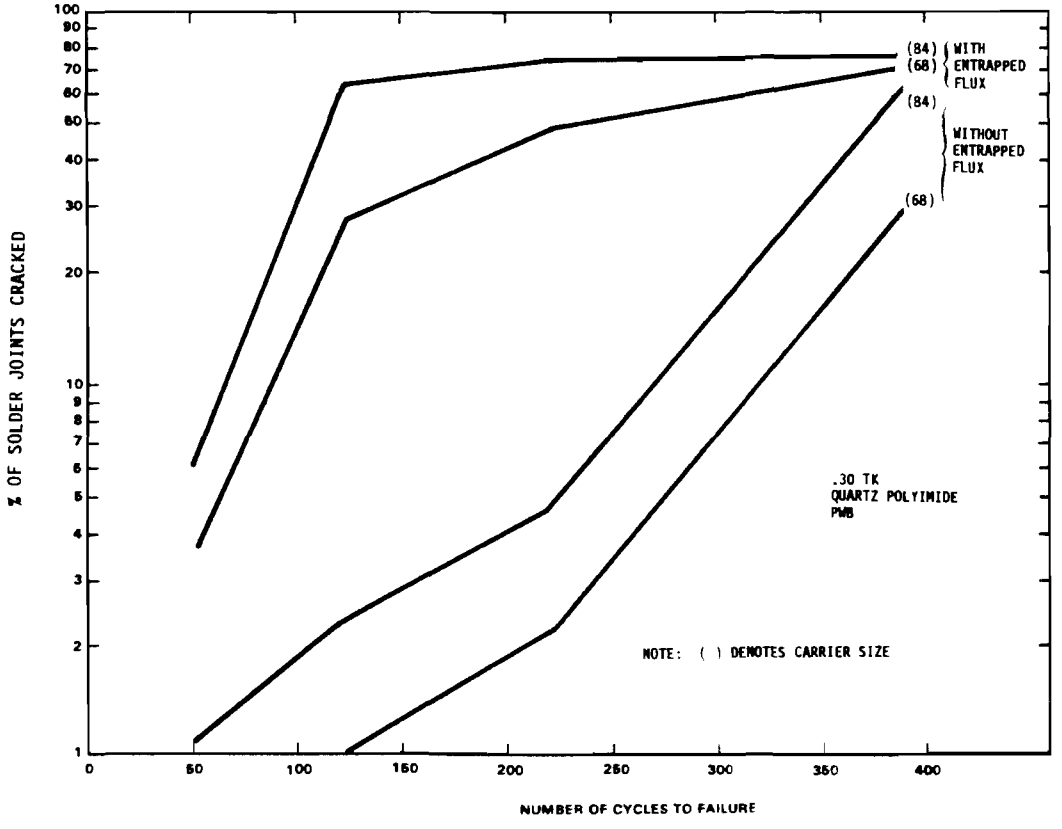


FIGURE 19:
COMPARISON OF PERCENT FAILED SOLDER JOINTS
VERSUS NUMBER OF CYCLES ON CARRIERS WITH AND
WITHOUT ENTRAPPED FLUX
(REF. #31)

Substrate Reliability

The primary failure mechanisms plaguing substrate reliability have traditionally been due to the plated through-holes required to accommodate inserted package leads. With the elimination of hole drilling for surface mount packaging and the size reduction in the holes drilled for thermal/electrical vias, surface mounted substrates have the potential for a corresponding increase in reliability.

The problems of mating materials with unlike thermal coefficient properties have been addressed at the board level. By manipulating substrate materials and constructions, the magnitude of the stress which develops in the solder joint has been substantially reduced.

Temperature profiles given in Figure 20 represent the nature of the TCE problem of the temperature differences which occur between the component and the substrate. The thermal mass of the component is much less than the thermal mass of the substrate which is responsible for the nonuniform heating during temperature cycling. The semiconductor operation of the component generates heat in the component package at a greater rate than the substrate during powered operation, and, therefore, the lag time of the substrate heating causes stress to develop in the solder bond which connects the component to the substrate.

Surface mount technology is influencing not only the types of packaging used but also the types of substrate materials. In the effort to alleviate the solder joint strain, the problem has been approached in a number of ways. Possible solutions to the stress buildup initiated by the unequal expansion of materials are as follows:

- Introduce a layer of compliant material between the PCB and component surface interfaces
- Develop a new PCB material
- Introduce a unique solder
- Establish a stress-resistant solder joint design
- Consider different package styles (i.e., plastic, leaded)

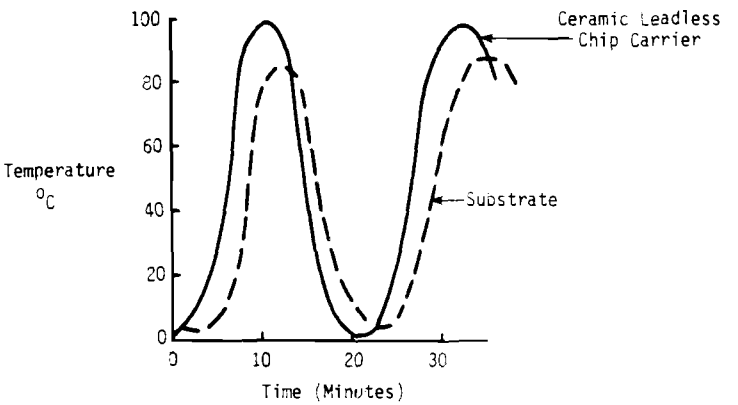


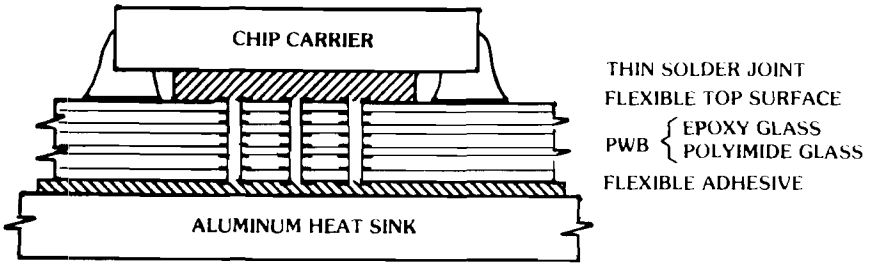
FIGURE 20:
TEMPERATURE CYCLING PRODUCES UNEQUAL
HEATING OF MATERIALS
(REF. #32)

Figures 21 through 23 show some of the different materials examined and methods explored in the search for the most cost - and performance-effective approach.

Flexible Top Layer

An approach to improve SMT reliability using a flexible top surface layer on the standard PWB is shown in Figure 21. The construction uses a flexible film on a standard PWB. Although the use of these materials showed the feasibility of using a compliant layer to reduce stress, there has been little pursuit of this approach.

By overall volume, the ceramic substrate is still the most widely used. This is a mature technology that has emerged as the industry standard but has proven to be limited in a number of ways. Even though the coefficient of thermal expansion is compatible to the ceramic component, the size of the substrate is limited by its weight, brittleness, expense and its lack of good electrical performance when using high-speed componentry.



ADVANTAGES

1. CLOSE TO MAINSTREAM PWB TECHNOLOGY
2. LOW COST
3. AVAILABLE TODAY

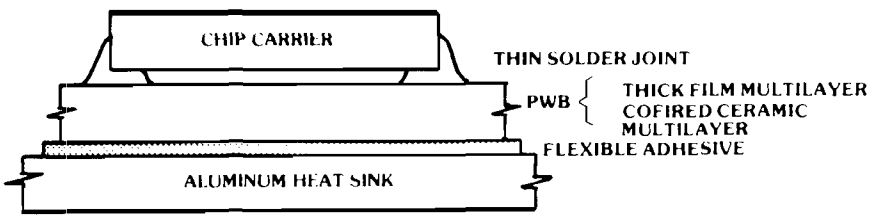
DISADVANTAGES

1. PROPRIETARY PROCESS
2. LIMITED TEST DATA AVAILABLE
3. WOULD NEED CONSIDERABLE DEVELOPMENT TO DEMONSTRATION PTH BARREL RELIABILITY

FIGURE 21:

UNCONSTRAINED APPROACH-FLEXIBLE TOP JOINT

(REF. #34)



ADVANTAGES

1. COMPATIBLE TCE WITH CHIP CARRIER
2. GOOD THERMAL CONDUCTIVITY
3. INDUSTRY STANDARD TODAY - MATURE TECHNOLOGY
4. GOOD PROCESS TECHNOLOGY
5. WIDE AVAILABILITY
6. COPPER THICK FILM COST COMPETITIVE IN SMALL SIZES

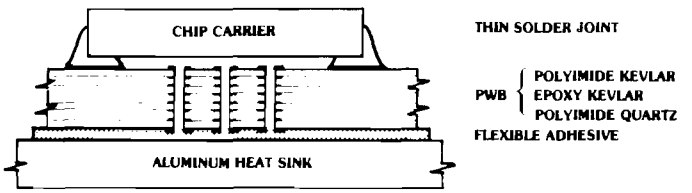
DISADVANTAGES

1. SIZE LIMITED TO 6x6 DUE TO WARP
2. 2 x ORGANIC COST USING PdAu
3. LIMITED REWORK POSSIBLE
4. CERAMIC SUBJECT TO FRACTURE IN MECHANICAL AND THERMAL SHOCK
5. HIGH DIELECTRIC CONSTANT

FIGURE 22:

CONSTRAINING DIELECTRIC SUBSTRATE-CERAMIC

(REF. #34)



ADVANTAGES

1. GOOD TCE MATCH TO CERAMIC
2. LARGE SUBSTRATE SIZE
3. PROCESSED WITH STANDARD PWB EQUIPMENT
4. TCE TAILORING POSSIBLE

DISADVANTAGES

1. RESIN CRACKS DUE TO ADHESION BETWEEN FIBER AND KEVLAR
2. SPECIAL DRILLING AND ROUTING PROCEDURES NEEDED
3. HIGH WATER ABSORPTION (KEVLAR)
4. EXPENSIVE RAW MATERIAL (KEVLAR)
5. FABRIC TOO THICK (THINNER MATERIALS IN DEVELOPMENT
6. LOW MODULES MATERIAL DRIVEN BY COPPER GROUND AND VOLTAGE PLANS

FIGURE 23:
CONSTRAINING DIELECTRIC SUBSTRATE-POLYMERIC
(REF. #34)

Constrained Dielectric

The use of a constraining layer to achieve the desired TCE characteristic has proven to be a popular approach. Different methods of using a constraining layer are:

- Copper Clad Invar Core has a low TCE which constrains the overall board expansion

- Layers of Copper Clad Invar Foil are sandwiched between standard epoxy-glass board materials which produce a good TCE and it is light-weight

- Kevlar Layers use standard epoxy-glass or polyimide-glass boards altered by replacing the fiberglass layer with a material having a low TCE such as Kevlar

Figure 24 compares the results obtained from thermal shock testing of a typical polyimide-glass board and a polymer/metal substrate (i.e., Invar/Copper) containing a 44-lead chip carrier (on 0.040 centers) as the largest device.

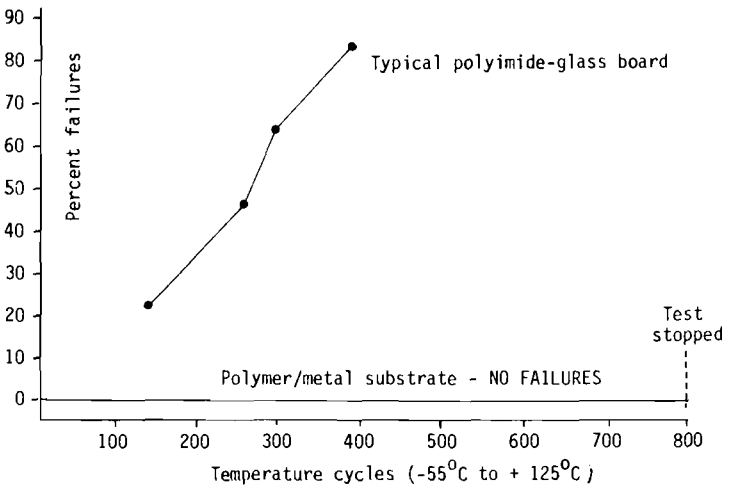


FIGURE 24:
THE RESULTS OF THE THERMAL SHOCK TESTS SHOW THAT A TYPICAL POLYIMIDE/GLASS BOARD FAILS AFTER SEVERAL HUNDRED CYCLES (REF. #23)

Regarding printed wiring board reliability, the use of SMT offers one distinct advantage over conventional DIP packaging; that is, the use of SMT dramatically reduces the need for plated through-holes. The only plated through-holes needed for an SMT assembly are "via" holes used to provide electrical and thermal connections between different interconnection layers. The number of holes (vias) will generally be greater for an SMT assembly. However, the total number of plated through-holes (i.e., vias plus holes for component leads) will be much fewer.

Recent test data (source proprietary) on SMT assemblies with TCE tailored substrates has indicated a large number of plated through-hole failures due to z-axis expansion problems. Apparently the TCE tailoring of the package and substrate has resulted in this unexpected problem. It is anticipated that the failure cause is process-related, specifically due to drilling and/or plating difficulties.

The number of plated through-holes has been the leading indicator of PWB reliability (Ref. #35). It has been observed that 98% of all PWB failures can be attributed to plated through-hole failures (Ref. #36). Therefore, the reduction of the required number of plated through-holes and the anticipated lower PWB failure rate can be used as an argument to support the use of SMT if the previously described process problems can be resolved.

SECTION 6: FAILURE RATE PREDICTION MODEL DEVELOPMENT

The use of surface mount technology affects the design of three different areas, namely the microcircuit package, solder connections and the printed wiring board. Corresponding MIL-HDBK-217 reliability prediction models need to be evaluated, refined and/or replaced to account for the reliability of the surface mount design. The existing MIL-HDBK-217 models were developed based primarily on conventional printed wiring and plated through-hole designs and therefore may not accurately predict the failure rate for equipments designed with surface mount technology. This section presents design-oriented SMT failure rate models and describes the reliability modeling performed to support the models. These models allow the equipment designer to study and evaluate the implications of using SMT.

The reliability modeling efforts performed to support this technical document individually investigated the microcircuit packages, the solder connections and printed wiring boards used for SMT. In many cases, it was difficult to specifically attribute the cause of failure. For example, an intermittent failure could be due to solder cracking (i.e., solder connection failure) or partial delamination of the printed wiring board trace (i.e., PWB failure). Given the available information, it can be difficult to precisely pinpoint the failure cause. In each case, the available failure documentation was examined and a determination was made.

Failure Rate Modeling Concepts

Failure rate prediction models ideally are developed based on statistical analysis of a large, balanced data set of documented field failures. For surface-mounted components, the preferred modeling approach of empirical data analysis was complemented by analysis of life

test data, physical failure mechanisms and theoretical and/or empirical reliability relationships presented in the literature. Development of reliability prediction models for surface mount technology is described in this section. Required assumptions are stated as they occur in the model development process.

It was necessary to emphasize test data, physics-of-failure information and published reliability relationships during the model development process. Use of statistical methods was somewhat limited due to the nature and quantity of the available data. Development of timely reliability prediction models often presents an intriguing paradox to the reliability analyst. Applicable and accurate reliability prediction models are required when an emerging technology initially sees widespread usage, and yet the data to develop the needed models will not be available until some time (i.e., several years) after the new technology is widely used. This paradox is particularly noticeable when the part-type or technology in question exhibits very low failure rates such as those observed for a surface-mounted connection soldered under tightly controlled conditions and stringent specifications. In these cases, the time to develop a sufficient data base can be fairly lengthy.

A general failure rate modeling approach was applied. This approach has been successfully applied by IITRI/RAC many times to develop reliability prediction models. The modeling approach is defined by the following tasks and subtasks:

Task 1: Theoretical Model Development
- 1.1 Literature Search
- 1.2 Variable Identification
- 1.3 Model Form Hypothesis

Task 2: Data Collection

Task 3: Statistical Analysis

3.1 Correlation Coefficient Analysis

3.2 Regression Analysis

3.3 Model Formation

The theoretical model development task consists of a literature search, the identification of potential failure rate model input parameters and the hypothesis of a model form. This task was intended to provide direction to the overall model development process, to provide the resultant prediction models with a strong theoretical foundation and to complement the data analysis task by compensating for data deficiencies. An overview of the theoretical model development subtasks is presented in the following paragraphs.

The variable identification subtask consisted of identifying part construction and application variables which characterize surface mount components in their operating state. Emphasis during the variable identification subtask was directed towards the identification of variables which would be accessible to prediction model users. Several variables which were thought to influence failure rate were rejected because they would not be known by the analyst performing the reliability prediction. For example, the package lead surface solderability or the solder joint ductility are important parameters affecting solder connection failure rate. However, their values are difficult to measure, and the anticipated increased accuracy provided by inclusion of these variables would be offset by decreased model usability.

The variables selected represent possible failure rate model input parameters. Separate lists of variables were identified for (1) microcircuit packages, (2) solder connections, and (3) printed wiring boards. These variables are presented in Tables 11, 12 and 13.

TABLE 11:

PACKAGE APPLICATION AND

CONSTRUCTION VARIABLES

Application - Power - Temperature (Ambient, Cycling) - Environment
Design - Thermal Resistance - Package Type - Lead Configuration - Package Dimensions
Complexity - Number of Pins

TABLE 12:

SOLDER CONNECTION APPLICATION AND

CONSTRUCTION VARIABLES

Application - Power - Temperature (Ambient, Cycling) - Environment
Process - Application Technique (Reflow, Wave, etc.) - Inspection - Process Controls
Design - Connection Dimensions (Stand-off Height, Fillet Angle) - Solder Composition - Surface Plating (PWB, Component Lead) - Package Type (Compliant Leads, Leadless, etc.)
Complexity - Number of Pins Per Device - Device Package Dimensions

TABLE 13:

PWB APPLICATION AND CONSTRUCTION VARIABLES

Application - Power - Temperature (Ambient, Cycling)
Design - Substrate Material - Thickness - Quality (IPC/MIL-Spec Standards)
Complexity - Number of Via Holes - Number of Circuit Planes (i.e., Layers) - Number of Board Connections

The next phase of the theoretical model development consisted of an in-depth evaluation of the anticipated failure mechanisms. The impact of the following factors were included as part of the theoretical model:

- Function
- Technology
  - Fabrication Techniques
  - Fabrication Process Maturity
- Failure Mode/Mechanism Experience
- Complexity
- Packaging Techniques
- Effectiveness of Process Controls
- Effectiveness of Screening and Test Techniques
- Environment and Temperature

Different failure rate model forms were considered and evaluated. Many documented relationships were found relating solder connection reliability to factors such as connection size and temperature. These relationships were included in the solder connection theoretical model

due to the general agreement between sources. For variables where there was no consensus of opinion or there was a general lack of information, all available information was studied and appropriate decisions were made. In certain instances, only a qualitative assessment could be made, thereby limiting the usefulness of the models. These models, however, are presented primarily as a design tool to enable the reliability engineer to judge the relative merits of SMT. The models presented in this document adequately serve this purpose and represent a comprehensive overview of available SMT reliability information.

The second major task was data collection. The RAC regularly pursues the collection of microcircuit and printed wiring board failure data. The most recent compilation of microcircuit failure data is presented in MDR-21A, "Microcircuit Device Reliability, Field Experience Database" (Ref. #37) dated Spring 1985, and printed wiring board data is presented in NPRD-3, "Nonelectronic Parts Reliability Data" (Ref. #38) dated Winter 1985/86.

These data resources, which had been collected and summarized prior to the initiation of this study, were available for analysis. However, the specialized nature of this report necessitated additional concentrated data collection activities. A survey of commercial, industrial and government organizations was conducted to aid the data collection efforts. Organizations contacted either manufactured, used or tested SMT products. Information requested included field experience data, preproduction and production tests, life test data and failure mode/mechanism information.

Factors contributing to data collection difficulties in general and for SMT specifically include:

- Difficulty in identifying specific failure cause
- Lack of accurate failure reporting systems
- Inability to precisely determine environmental and operational stresses on the devices
- Omission of many equipment operators to accurately record the amount of operating hours and on/off power cycling

These problems limited the use of field data. However, some data were available for analysis. Additionally, much research has been performed to evaluate and improve the use of surface mount technology. The available field reliability data together with the documented research provided sufficient information to develop initial reliability prediction models. As more data becomes available, the models should be refined and quantified to reflect additional technological enhancements and to take advantage of greater data resources.

The final major subtask is data analysis and model formation. Practical data analysis techniques are used together with engineering and physics-of-failure information to yield accurate models which are sensitive to known failure-accelerating stresses. Statistical analyses for reliability engineers are described in detail in SOAR-2, "Practical Statistical Analysis for the Reliability Engineer," (Ref. #55) dated Spring 1983.

Device Packages

The RAC microcircuit data base was complemented with an in-depth assessment of anticipated failure mechanisms to develop proposed revisions to the MIL-HDBK-217 monolithic microcircuit models. This section of the technical report describes the procedure followed and presents the recommendations.

It was not the objective of this study to independently determine unique models for surface-mounted microcircuits. Instead, it was intended to evaluate the existing series of microcircuit models, identify inadequacies with the existing models regarding SMT and to quantify the required package-related refinements. To accomplish these goals, the RAC data base was queried for flatpack devices, leaded chip carriers and leadless chip carriers. This data is presented in Appendix B.

The existing series of MIL-HDBK-217 microcircuit models is generally of the following form:

$$\lambda_p = \pi_Q [C_1 \pi_T + (C_2 + C_3) \pi_E)]$$

where:

λ_p = device failure rate (failures/10^6 hours)
π_Q = quality factor
C_1, C_2 = circuit complexity factors
C_3 = package complexity factor
π_T = temperature factor
π_E = environmental factor

It is necessary to evaluate the existing model in regard to SMT to identify missing factors and to determine the relevance of existing factors. The primary conclusion from this task has been the identification of two factors, temperature factor (π_T) and package complexity factor (C_3), which are not appropriate for predicting the failure rate of SMCs. A secondary conclusion is that the microcircuit quality factor (π_Q) is not currently sensitive to SMT packaging considerations.

The existing temperature factors are inappropriate because the heat dissipation properties are different for the smaller-dimension surface mount packages. It is anticipated that the heat-dissipation properties of SMCs will potentially manifest themselves in the form of higher device failure rates as temperature rises. The other conflict with the existing models is the package complexity factor (C_3). The C_3 factor does not include options for leaded or leadless chip carrier packages which renders the existing models unusable for SMT devices in those package types.

The issue of the microcircuit temperature factor is resolved simply by the determination of the appropriate thermal resistance properties for SMT. The table in MIL-HDBK-217, Section 5.1.2.5 which provides typical thermal resistance values needs to be updated to provide thermal resistance values for SMCs. Table 14 presents typical junction-to-case (θ_{JC}) and junction-to-ambient (θ_{JA}) thermal resistance values for leaded and leadless chip carriers.

TABLE 14:

SMT THERMAL RESISTANCE VALUES

Device Description	Number of Pins	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Reference
CLCC	20	166	-	39
CLCC	44	94	-	39
CLCC	52	61	-	39
CLCC	132	-	10.8	40
PLCC	20	113.6	37.1	41
PLCC	28	76.8	32.2	41
PLCC	44	68.0	20.3	41
PLCC	68	45.7	11.4	41

Notes: (1) CLCC = Ceramic Leadless Chip Carrier
(2) PLCC = Plastic Leaded Chip Carrier

The issue of the C_3 factor was investigated by analyzing RAC life and field microcircuit failure data for leaded and leadless chip carriers. An appropriate C_3 factor for flatpack packages is already included in MIL-HDBK-217 and was not studied here.

The additive form of the MIL-HDBK-217 microcircuit model is designed to partition the device failure rate between package-related failures and circuit-related failures. This model form assumes that the majority of package-related failure mechanisms are predominantly accelerated by environmental stresses and that the majority of die-related mechanisms are accelerated by temperature.

Thus, the model can be broken into its two basic constituate parts:

$$\lambda_{package} = C_3 \pi Q \pi E$$

$$\lambda_{die} = C_1 \pi Q \pi T$$

The C_2 circuit complexity term was not considered because its contribution is generally negligible in comparison with C_3.

To determine a unique C_3 relationship as a function of the number of pins, RAC-observed failure rates were substituted into the equation for package failure rate. The package failure rate was distinguished from the total device failure rate according to the documented "failure location" data at RAC. Table 15 presents the percentage of total device failures attributed to the package. Observed failure rates were multiplied by these percentages to determine package failure rates. Solving for C_3 then results in:

$$C_3 = \frac{\lambda \text{ package}}{\pi_Q \ \pi_E}$$

TABLE 15:
DISTRIBUTION OF PACKAGE FAILURES

Device Category	Hermetic	Nonhermmetic
Digital	60.9	47.2
Linear & Interface	19.9	23.7
Memory	5.3	20.3
VLSI	7.1	14.3

RAC data (presented in Appendix B) with observed failures was used to compute C_3 values. Linear regression was then applied to the data to relate C_3 to the number of pins. The best-fit regression solution was determined using least-squares. However, this trend was not statistically significant. The lack of correlation was attributed to one of the three following reasons:

(1) Pin count does not affect failure rate.

(2) There was insufficient data (seven data entries) to detect any apparent effect.

(3) The statistical "noise" inherent with failure rate masked the effect of pin count.

It was not possible to identify which of these specific explanations accounted for the lack of correlation. Intuitively, pin count does affect package failure rate and cannot be discounted. As a final modeling action, a C_3 relationship was forced through the data to be consistent with the existing C_3 relationships. The resulting equation is design-oriented and provides the relative relationship between failure rate, pin count and package type.

To determine the forced C_3 relationship for leaded and leadless chip carriers, it was assumed that the factor exponent was equal to the existing exponent for flatpacks. The forced relationship is given by:

$$C_3 = 8.28 \times 10^{-5} (N_p)^{1.82}$$

where:

N_p = number of pins

Conclusions from this investigation of SMT packages were that:

- thermal resistance needs to be reevaluated
- package complexity factor needs to be expanded

A secondary conclusion from the microcircuit package investigation was that the quality factor may need to be reassessed for SMT package types. Currently, there is a single series of quality factors for all microcircuit part types. Clearly, screening impacts the rate of occurrence of package-related failures. It is therefore recommended

that further investigations be concerned with the sensitivity of the quality factor to package-related variables.

The forced C_3 relationship is useful as a tentative factor to improve the utility of the microcircuit models. The forced factor was based on field failure data and, on average, provides accurate failure rate predictions.

Solder Connections

The study of SMT solder connection reliability is probably the most controversial and most interesting aspect of SMT. A review of the References section of this document reveals an abundance of technical research in this area. Additionally, the available literature often cited the results of reliability testing and, in several instances, the results of field operation. The documented reliability relationships found in the literature were used together with the available failure data to determine a failure rate prediction model for SMT solder connections. SMT solder connection reliability testing data is presented in Table 16.

Much of the technical research regarding SMT solder connections was concerned with empirical validation or modifications of the Coffin-Manson model (Ref. #42) of high-temperature, low-cycle fatigue. The Coffin-Manson model is intended to relate the number-of-cycles-to-failure to the plastic strain range. The plastic strain range depends on several factors including temperature levels, solder joint dimensions, solder material and substrate material. The most dominant variable is generally believed to be the differential in TCE between the substrate and the device package. The unmodifed Coffin-Manson model is given by the following equation:

$$\Delta\varepsilon_p = C(N_f)^{-\beta}$$

where:

$\Delta\varepsilon_p$ = plastic strain range
N_f = number of cycles to failure
C, β = constants

The literature includes many attempts to modify the basic Coffin-Manson model for specific SMT applications or interests. Several of these modified model forms were studied to support the model development effort and are discussed in the following paragraphs.

TABLE 16:
SMT FAILURE DATA

Ref. #	Failures	Total Cycles (1)	Mean Cycles to Failure	Remarks	Test Conditions
43	0	2,304,000 Connection	>2,304,000	24-pin plastic leaded chip carrier	Temperature Cycling: 0 to +100°C Failures defined as open circuits
	0	1,680,000 Connection	>1,680,000	28-pin plastic leaded chip carrier	
	2(2)	4,080,000 Connection	2,040,000	68-pin plastic leaded chip carrier	
44	1(2)	8,400 Connection	8,400	Epoxy-glass substrate, 28-pin hermetic chip carrier	Temperature Cycling: -55 to +125°C Cycle: Dwell time of 1 hour Total of 1000 cycles performed
	0	28,000 Connection	>28,000	Copper-Invar substrate, 28-pin hermetic chip carrier	
	1(2)	8,800 Connection	8,800	Epoxy/glass substrate, 44-pin hermetic chip carrier	
	0	44,000 Connection	>44,000	Copper-Invar substrate, 44-pin hermetic chip carrier	
	0	68,000 Connection	>68,000	Epoxy/glass substrate, 68-pin hermetic chip carrier	
	1(2)	8,400 Connection	8,400	Epoxy/glass substrate, 84-pin hermetic chip carrier	
	0	8,400 Connection	>8,400	Copper-Invar substrate, 84-pin hermetic chip carrier	
45	N/A	N/A	15-100 Connection	Pretinned ceramic leadless chip carrier	Temperature Cycling: -65 to +150°C MIL-STD-883, Method 1010, Test Condition C
	N/A	N/A	220-375 Connection	Cermamic leadless chip carrier (not pretinned) with small solder fillet	
	N/A	N/A	>720 Connection	Ceramic leadless chip carrier with solder post	

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean Cycles to Failure	Remarks	Test Conditions
31	N/A	N/A	18,000 Connection	Epoxy fiberglass substrate, 20-pin leadless chip carrier	Temperature Cycling: 0 to +85°C
	N/A	N/A	24,000 Connection	Polyimide fiberglass substrate, 20-pin leadless chip carrier	
	N/A	N/A	78,000 Connection	Polyimide PWB/Cu-Invar Core, 20-pin leadless chip carrier	
	N/A	N/A	140,000 Connection	Kevlar PWB, 20-pin leadless chip carrier	
	N/A	N/A	400,000 Connection	Cu-Invar Epoxy fiberglass PWB, 20-pin leadless chip carrier	
	N/A	N/A	11,200 Connection	Epoxy fiberglass substrate, 20-pin leadless chip carrier	Temperature Cycling: -40 to +71°C
	N/A	N/A	14,000 Connection	Polyimide fiberglass substrate, 20-pin leadless chip carrier	
	N/A	N/A	48,000 Connection	Polyimide PWB/Cu-Invar Core, 20-pin leadless chip carrier	
	N/A	N/A	80,000 Connection	Kevlar PWB, 20-pin leadless chip carrier	
	N/A	N/A	260,000 Connection	Cu-Invar Epoxy fiberglass PWB, 20-pin leadless chip carrier	

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean Cycles Failure	Remarks	Test Conditions
31	N/A	N/A	3,800 Connection	Epoxy fiberglass substrate, 20-pin leadless chip carrier	Temperature Cycling: -55 to +125°C
	N/A	N/A	5,000 Connection	Polyimide fiberglass substrate, 20-pin leadless chip carrier	
	N/A	N/A	18,000 Connection	Polyimide PWB/Cu-Invar Core, 20-pin leadless chip carrier	
	N/A	N/A	32,000 Connection	Kevlar PWB, 20-pin leadless chip carrier	
	N/A	N/A	80,000 Connection	Cu-Invar Epoxy fiberglass PWB, 20-pin leadless chip carrier	
1	0	800 PWB	>800	4-layer Copper-Invar-Copper/Polyimide board, 44-pad ceramic leadless CC (largest package)	Temperature Cycling: -55 to +125°C
	0	1,500 PWB	>1,500	4-layer Copper-Invar-Copper/Epoxy board, 64-pad ceramic leadless CC (largest package)	
	0	400 PWB	>400	1-layer Copper-Invar-Copper/Porcelain board, 68-pad ceramic leadless CC (largest package)	
	0	1,000 PWB	>1,000	1-layer Copper-Invar-Copper/Epoxy board, 84-pad ceramic leadless CC (largest package)	
	1	3,328,000 Connection	3,328,000	3-layer Copper-Invar-Copper/Polyimide board, 68-pad ceramic leadless CC (largest package)	Temperature Cycling: -34 to +71°C
	0	700 PWB	>700	3-layer Copper-Invar-Copper/Polyimide board, 68-pad ceramic leadless CC (largest package)	Temperature Cycling: -40 to +85°C

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean Cycles to Failure	Remarks	Test Conditions
1	0	1,000 PWB	>1,000	1-layer Copper-Invar-Copper/ Epoxy board, 84-pad ceramic leadless CC (Largest package)	Temperature Cycling: -55 to +125°C
	0	1,000 PWB	>1,000	1-layer Copper-Invar-Copper/ Epoxy board, 84-pad ceramic leadless CC (largest package)	
	0	1,000 PWB	>1,000	3-layer Epoxy glass elastomer board, 52-pad ceramic leadless CC (largest package)	
	0	1,000 PWB	>1,000	3-layer Epoxy glass elastomer board, 52-pad ceramic leadless CC (largest package)	
	0	500 PWB	>500	4-layer Polyimide/Kevlar board, 64-pad ceramic leadless CC (largest package)	Temperature Cycling: -40 to +87°C
	0	1,000 PWB	>1,000	8-layer Epoxy Kevlar board, 84-pad ceramic leadless CC (largest package)	Temperature Cycling: -65 to +125°C
	0	500 PWB	>500	6-layer Polyimide Kevlar on Copper-Invar-Copper Metal board, 84-pad ceramic leadless CC (largest package)	Temperature Cycling: -55 to +125°C

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean Cycles to Failure	Remarks	Test Conditions
46	2(3)	135 Package	68	Thick-film substrate pad lifting; cracking between metallized pad and dielectric	Temperature Cycling: -55 to +125°C Test Conditions: MIL-STD-202, Method 107
	3(4)	30 Package	10	Cracking between solder and LCC castellation; cracking in LCC metallized pads	
	1(4)	1,100 Package	1,100	Cracking in the LCC metallized pads	Temperature Cycling: +20 to +125°C
47	58	236,000 Package	4,069	24-lead premolded chip carrier	Humidity/Environmental Test: -85°C/85% RH 40 vdc/ground - biasing on alternate pins
48	1	1,560,000 Connection	1,560,000	40 and 64-pin pin (ceramic) chip carriers	Power Cycling at 60°C (ambient) with power on for 2.5 minutes and off for 2.5 minutes, all joints subjected to 500 cycles for each interval - 1.0W, 1.4W, 1.8W, 2.2W, 2.6W, 3.0W
2	.082(5)	600 Package	7,020	Thick film on alumina ceramic substrate, leadless ceramic chip carriers ranging in size from 24 to 64 leads	Temperature Cycling: -55 to +125°C Total of 600 cycles performed
	.099(5)	600 Package	5,760	Thick film on porcelain/steel substrate, leadless ceramic chip carriers ranging in size from 24 to 64 leads	
	.300(5)	600 Package	1,700	Microwire polyimide on Alloy-42 substrate, leadless ceramic chip carriers ranging in size from 24 to 64 leads	
	.420(5)	600 Package	1,130	Polyimide/glass substrate, leadless ceramic chip carriers ranging in size from 24 to 64 leads	

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean Cycles to Failure	Remarks	Test Conditions
49	0(3)	1,260,000 Connection	>1,260,000	Alumina substrate with 10-mil solder deposition for components with 20, 28 & 40 pins	Temperature Cycling: -55 to +125°C MIL-STD-883, Method 1010, Test Condition B Dwell time of 83 minutes Total of 550 cycles performed
	71(3)	1,634,275 Connection	23,020	Polyimide fiberglass substrate with 10-mil solder deposition for components with 20, 28 & 44 pins	
	27(3)	727,900 Connection	26,959	Polyimide fiberglass substrate with 20-mil solder deposition for components with 20, 28 & 44 pins	
	39(3)	610,425 Connection	15,652	Polyimide fiberglass substrate with 20-mil solder deposition for components with 20, 28 & 44 pins	
34	10(2)	452,531 Connection	45,253	Epoxy/Copper-Invar-Copper/Epoxy substrate construction, 68 and 84-pin LCCs on 0.050 centers	Temperature Cycle Testing: -55 to +125°C 5-minute ambient recovery between temperature extremes Tested every 50 cycles
	14(2)	170,827 Connection	12,202	Polyimide/Copper-Invar-Copper/Polyimide substrate construction, 68 and 84-pin LCCs on 0.050 centers	Circuit considered failed (open) if resistance 200 ohms at ambient temperature

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean Cycles to Failure	Remarks	Test Conditions
16	4(3)	114,230 Connection	28,558	29 Ceramic substrates, each populated with 4 components: (1) 24-lead, (2) 32-lead, (1) 48-lead, (1) 64-lead	Temperature Cycling: -55 to +125°C MIL-STD-202F, Method 1071, Test Condition B 25 minutes at each temperature extreme and 5 minutes at 25°C between temperature extremes Total of 600 cycles performed 50 mA of current biasing per board
	22(3)	59,572 Connection	2,708	43 Porcelain steel substrates, each populated with 4 components: (1) 24 lead, (1) 32-lead, (1) 48-lead, (1) 64-lead	
	7(3)	22,423 Connection	3,203	Two Polyimide substrates, each populated with 4 components: (1) 24-lead, (1) 32-lead, (1) 48-lead, (1) 64-lead	
	2(3)	28,150 Connection	14,075	12 Alloy 42 substrates, each populated with 4 components: (1) 24-lead, (1) 32-lead, (1) 48-lead, (1) 64-lead	
	0(3)	28,800 Connection	>28,800	12 Copper-Invar substrates, each populated with 4 components: (1) 24-lead, (1) 32-lead, (1) 48-lead, (1) 64-lead	
50	38(4)	3,766,700 Connection	99,124	Copper-Invar-Copper substrate populated with 25 of each package type, 20-pin, 44-pin, 68-pin, 84-pin	Temperature Cycling: -55 to +100°C 30 minutes at each temperature extreme Total of 700 cycles performed Failure defined as solder joint crack in 50% of solder contour
	0(2)	3,780,000 Connection	>3,780,000	Copper-Invar-Copper substrate populated with 25 of each package type, 20-pin, 44-pin, 68-pin, 84-pin	
	2(2)	4,859,100 Connection	2,429,550	Copper-Invar-Copper substrates populated with 25 of each package type, 20-pin, 44-pin, 68-pin, 84-pin	Temperature Cycling: -55 to +100°C 30 minutes at each temperature extreme Total of 900 cycles performed Failure defined as solder joint crack in 50% of solder contour
	63(4)	4,810,500 Connection	76,357	Copper-Invar-Copper substrate populated with 25 of each package type, 20-pin, 44-pin, 68-pin, 84-pin	

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean Cycles to Failure	Remarks	Test Conditions
8	3(2)	240,000 Connection	80,000	Glass/Polyimide substrate populated with 10 40-pin devices	Temperature Shock: -55 to +125°C (liquid to liquid) Failure defined as an increase in electrical resistance
	2(2)	1,059,840 Connection	529,920	Glass/Polyimide substrate	
28	6(2,4)	82,133 Connection	13,689	Epoxy-glass substrate, 40-mil leadless packages of 6 sizes: (1) 16-pin, (1) 20-pin, (1) 32-pin, (1) 40-pin, (1) 64-pin, (1) 84-pin	Temperature Cycling: -55 to +125°C MIL-STD-883B, Method 1014.4 5-volt biasing on input pins Dwell time of 45 minutes with 15 minutes of each temperature extreme. Total of 100 cycles performed Failures are defined as open circuits due to cracks formed on the surface and at the base of the solder joint
	6(2,4)	131,840 Connection	21,973	Polyimide-glass substrate, 40-mil leadless packages of 6 sizes: (1) 16-pin, (1) 20-pin, (1) 32-pin, (1) 40-pin, (1) 64-pin, (1) 84-pin	
	6(2,4)	174,293 Connection	29,049	Polyimide-quartz substrate, 50-mil leadless packages of 6 sizes: (1) 16-pin, (1) 20-pin, (1) 32-pin, (1) 40-pin, (1) 64-pin, (1) 84-pin	
	6(2,4)	105,813 Connection	17,636	Epoxy-glass substrate, mil-50 leadless packages of 6 sizes: (1) 16-pin, (1) 20-pin, (1) 32-pin, (1) 40-pin, (1) 64-pin, (1) 84-pin	
	6(2,4)	117,333 Connection	19,556	Polyimide-glass substrate, 50-mil leadless packages of 6 sizes: (1) 16-pin, (1) 20-pin, (1) 32-pin, (1) 40-pin, (1) 64-pin, (1) 84-pin	
	6(2,4)	188,800 Connection	31,467	Polyimide-quartz substrate, 40-mil leadless packages of 6 sizes: (1) 16-pin, (1) 20-pin, (1) 32-pin, (1) 40-pin, (1) 64-pin, (1) 84-pin	

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean to Cycles Failure	Remarks	Test Conditions
39	0	1,032,400 Connection	>1,032,400	Epoxy-glass and enriched resin substrate, ceramic leadless chip carriers of 3 sizes: 20-lead, 44-lead, 52-lead	Temperature Cycling: -55 to +125°C MIL-STD-883B, Method 1010.3, Test Condition B 15 minute soak at each all temperature extreme with a transition time of 5 minutes between temperature extremes
	8	226,200 Connection	28,275	Epoxy-glass substrate, ceramic leadless chip carriers of 3 sizes: 20-lead, 44-lead, 52-lead	
	2	475,600 Connection	237,800	Polyimide and enriched resin substrate, ceramic leadless chip carrier of 3 sizes: 20-lead, 44-lead, 52-lead	
	8	359,600 Connection	44,950	Polyimide substrate, ceramic leadless chip carriers of 3 sizes: 20-lead, 44-lead, 52-lead	
	12	174,000 Connection	14,500	Single thick-layer Epoxy-glass substrate, ceramic leadless chip carriers of 3 sizes: 20-lead, 44-lead, 52-lead	
	7	533,600 Connection	76,229	Substrate with compliant elastomer surface, ceramic leadless chip carriers of 3 sizes: 20-lead, 44-lead, 52-lead	
	6	278,400 Connection	46,400	Non-compliant surface substrate with low TCE, ceramic leadless chip carriers of 3 sizes: 20-lead, 44-lead, 52-lead	

TABLE 16:
SMT FAILURE DATA (CONT'D)

Ref. #	Failures	Total Cycles (1)	Mean Cycles to Failure	Remarks	Test Conditions
41	0	1,800,000 Connection	>1,800,000	20-pin plastic chip carrier on 50-mil centers	Temperature Cycling: -65 to +150°C
	0	760,000 Connection	>760,000	20-pin plastic chip carrier on 50-mil centers	Temperature Shock: -65 to +150°C

Notes: (1) Total cycles is provided to the lowest level possible. If all requisite information is available, connection cycles is provided (connection cycles = (test cycles) x (No. of connections per test). If the number of connections per package is unknown, package cycles (package cycles = (test cycles) x (No. of packages per test) is provided. If the number of packages is unknown, PWB cycles is provided (PWB cycles = (test cycles) x (No. of PWBs per test). In each instance, the appropriate units are designed under the cycles quantity.

(2) Electrical test failure

(3) Substrate/solder interface connection failure

(4) Package/solder interface connection failure

(5) Fraction of failed connections given (actual number of failed connections unknown)

The effects of power cycling frequency was studied (Ref. #51), resulting in the following modified model. This model represents an attempt to model high-temperature creep and corrosion failure mechanisms:

$$\Delta\varepsilon_p = C(N_f(\nu)^{k-1})^{-\beta}$$

where:

ν = power cycling frequency
k = constant

Temperature was factored into the solder connection life-prediction model in Ref. #52. In this research, the cycles-to-failure was related to temperature by assuming an equivalent Arrhenius relationship. The modified model presented was given by:

$$N_f = C(\nu).^{33}(\Delta\delta)^{-2}\, e^{(-E/KT)}$$

where:

$\Delta\delta$ = shear strain range
K = Boltzman's constant
T = temperature (^{o}K)
E = constant

Bell Laboratories (Ref. #29) also worked to advance the study of SMT solder connection reliability. Another modified form of the Coffin-Manson model was presented as:

$$N_f = 0.5\ \left[\frac{F\ \Delta\delta}{2\ \varepsilon_f}\right]^{1/c}$$

where:

ε_f = fatigue ductility coefficient
c = fatigue ductility exponent
F = constant

In general, the above-mentioned research and references included empirical estimates of the model constants. These technical articles are again referenced to the reader who is interested in obtaining more detailed information.

Clatterbaugh and Charles (Ref. #53) described a testing program to evaluate the effectiveness of unmodified and modified Coffin-Manson relationships. A significant conclusion from this research was that the solder joint dimensions are an extremely important factor for SMT solder connection reliability. The effect of solder joint dimensions (stand-off height, fillet angle) is not adequately represented by the previously described research. Solder joint dimensions were implicitly included in these models by the plastic strain range and the shear strain range.

Research encompassing solder joint dimensions explicitly is described by Engelmaier (Ref. #54). The result of this research is the following modified Coffin-Manson model.

$$N_f = 0.5 \left[\frac{2h\ (2\varepsilon f)}{L_{max}\ \Delta\varepsilon_{max}}\right]^{-1/c}$$

where:

h = solder joint height
L_{max} = maximum linear distance between corner solder joints
$\Delta\varepsilon_{max}$ = maximum expansion differential

A study of SMT solder connection reliability requires an investigation of the time-dependent nature of solder connection failure rate. There was insufficient documented time-to-failure data to properly investigate failure rate time-dependance. However, the cumulative nature of solder connection fracture and fatigue would tend to eliminate the popular exponential distribution (i.e., constant failure rate) from contention. It is much more likely that the log-normal distribution applies to solder connection failure rate. This has been supported in the literature (Ref. #56).

The available data and the documented research provides sufficient information to develop and propose a design-oriented reliability prediction model. To properly characterize the log-normal distribution, the mean and the standard deviation must be estimated. The standard deviation is highly process-related, and it is inappropriate to provide models to predict the standard deviation without in-depth evaluation, standardization and quantification of process controls and methods. The appropriate model for the SMT solder connection mean-time-to-failure was found to be:

$$MTTF = \tau_b \pi_h \pi_{ccs} \pi_E \left[\frac{1}{aN_1 + bN_2}\right]$$

where:

MTTF = solder connection mean-time-to-failure (hours)

τ_b = base time to failure (based on substrate material)
- = 3.3, epoxy/glass
- = 440, copper clad invar
- = 730, ceramic

π_h = solder dimension factor
- = $(h)^{2.4}$ where h = stand-off height (mils.)

π_{ccs} = chip carrier size factor
- = $.69(L)^{-2.29}$ where L = chip carrier edge size (inches)

π_E = environmental factor

N_1 = number of power cycles per hour

N_2 = number of environment-related temperature cycles per hour

a = power constant, based on TCE tailoring

b = environment constant, based on ΔT

Solder connection reliability was defined based on the number of power-related and environment-related temperature cycling rates. There is a distinct difference between the two effects. The impact on solder connection MTTF of environment-related temperature cycling primarily depends on two factors:

(1) the temperature difference between high and low temperatures

(2) the TCE difference between package and substrate materials

The effect of power-related temperature cycling differs due to the localized heating associated with the applied power. The extent of the power cycling effect depends on TCE tailoring.

The environment constant (b) is based on the temperature differential between high and low temperatures (ΔT), or twice the amplitude of the temperature-cycling spectrum. It must be remembered that the difference in TCE was accounted for by the "base-mean-time-to-failure." Previous research (Ref. #31) indicates that the relationship between cycles to failure and ΔT is given by the following relationship. To support this relationship, testing was performed and data analyzed for a wide range of substrate materials and testing conditions.

$$\text{Cycles-to-failure} \propto (\Delta T)^{-2.0}$$

As a tentative factor, this relationship can be used to estimate 'b' values. The appropriate equation for 'b' is given by:

$$b = (\Delta T/25)+2.0$$

The power constant (a) is dependent on the extent of TCE tailoring. For a given combination of design-related variables (i.e., chip carrier dimensions, power levels, etc.), it is advisable to tailor the substrate material and even the choice of lead configuration to minimize the deleterious effects of power cycling. Intuitively, this factor depends on the substrate material, the package material, the applied power, the chip carrier dimensions and the lead configuration. As the extent of TCE tailoring increases, the magnitude of the power constant will decrease. Determination of precise values for the 'a' constant should be based on data analysis from a dedicated testing program to investigate SMT TCE tailoring. On average, the power constant will assume a value of one.

It is interesting to note that the size of the chip carrier is a significant factor in the solder connection failure rate. The chip carrier size factor was defined as a function of the edge size or width. It could also have been defined based on the surface area without changing the resultant predictions. The chip carrier dimensions have a pronounced effect on the translation of stress through the solder connection, and this is the expected result. For surface mount devices other than chip carriers, this factor assumes a value of one.

More research and active data collection is required to finalize the failure rate prediction model for SMT solder connections. However, the proposed model represents a meaningful step in the advancement of SMT reliability assessment.

Printed Wiring Boards

The dominant failure mechanisms for PWBs has historically been related to 360° plated through-hole (PTH) barrel cracks and fractures between surface or internal circuit paths and the PTH. The use of SMT greatly reduces the required number of PTHs and thereby intuitively reduces the PWB failure rate. Several other interesting effects are introduced by the advent of SMT. First, the typical number of via holes, used to provide electrical continuity between circuit layers, will be greater for SMT. Second, the use of SMT has caused a reassessment of the optimal substrate material chosen for specific applications. This also affects PWB reliability since the difference in thermal coefficients of expansion (TCE) between the substrate material and the copper PTH plating is the critical factor related to PTH fractures. These factors were explored as part of the PWB failure rate modeling process. Formal reliability modeling was not possible for PWBs because of a lack of failure data. However, conceptual models were developed and are presented in this section.

Initially, numerous potential variables were identified and considered. Variables were individually evaluated to determine (1) the theoretical or anticipated impact on failure and (2) the applicability for failure rate prediction modeling purposes. Several variables were eliminated from subsequent analysis based on both criteria. Variables which were eliminated include PWB foil weight, PTH plating thickness and many PWB manufacturing/processing variables.

The hypothesized PWB model form was designed to accomodate SMT, traditional DIP packaging and combinations of both. The model assumes the exponential reliability distribution despite several reservations concerning the cumulative nature of PTH damage. The hypothesized model is as follows:

$$\lambda_p = (\lambda_1 N_1 + \lambda_2 N_2 + \lambda_3 N_3)\, \pi_C\, \pi_Q\, \pi_E$$

where:

λ_p = PWB failure rate (failures/10^6 hours)
λ_1 = via PTH base failure rate
λ_2 = loaded PTH base failure rate
λ_3 = SMT proportionality constant
N_1 = number of via PTHs
N_2 = number of loaded PTHs
N_3 = number of surface mount connections
π_C = complexity factor (based on the number of circuit planes)
π_Q = quality factor
π_E = environment factor

Several variables were thought to influence failure rate but were not included in the hypothesized model. Most notable among these are the spacing between PWB traces and the application temperature. It seems intuitively appealing to include the spacing distance between conductor traces. This factor was not included, however, based on documented reseach (Ref. #57) which indicates that the effect of conductor spacing is minimal until a level approaching 3 mils. High temperature and temperature cycling cause distinct failure mechanisms. Ambient temperature was not included due to the dominant effect of temperature cycling (reflected by the environmental factor). In comparison, the effect of ambient temperature was considered to be smaller.

All three base failure rate constants (λ_1, λ_2, λ_3) and the environmental factor were defined as a function of board material. The sensitivity of the PWB failure rate to temperature cycling depends on the difference between the thermal coefficient of expansion of the substrate material and the copper PTH plating. As the number and the magnitude of the temperature cycles increase, the relative failure rate difference between board materials should also increase; that is, the rate of change for failure rate as a function of temperature cycling will be different based on the board material. The precise magnitude and frequency of temperature cycling is rarely known in the equipment design phase when predictions are performed. Therefore, this effect must be accounted for by the environmental factor, which groups mission profiles with similar environmental stress.

The three base failure rate constants are based on the substrate material for two reasons. First, it is necessary to scale the failure rates because the "ranges" of failure rate values are expected to be different for one or more of the available substrate material options. Another reason is to account for substrate material effects independent of the difference in TCE, most notably the surface smoothness after board drilling. A level but thin plating on a rough barrel wall will result in localized stress concentrations accelerating the failure process. This is potentially a major problem for PTHs in PWBs tailored for SMT applications.

The hypothesized model form is a combination of additive and multiplicative forms. There are several reasons for the additive form. The via PTHs, the loaded PTHs and the surface mount connections are physically separated on the PWB real estate. The rate of failure of the individual PTHs and SMT connections are independent and are thus additive in nature. It is necessary to segregate the unloaded (vias) and loaded PTHs because the presence of the component lead and corresponding solder connections significantly affects the translation of mechanical stresses throughout the PTH. Additionally, PTH dimensions tend to be different for via and loaded PTHs due to the differing design functions. The third base failure rate constant (λ_3) was defined as an SMT proportionality constant. This is intended to model PWB failures associated with the substrate-trace interface and was assumed to be proportional to the total number of surface mount connections.

The complexity factor was defined as a function of the number of circuit planes in a multilayer board. This quantity includes ground and voltage planes. Previous IIT Research Institute (IITRI) research (Ref. #35) indicated that a complexity factor can be represented by the following equation:

$$\pi_C = .65\ (L)^{.63}$$

where:

L = number of circuit planes

More dedicated and thorough research is required to collect PWB failure data for SMT assemblies to evaluate this relationship. As a preliminary relationship, this complexity factor is proposed for SMT.

Quantification of the PWB model requires the collection and analysis of observed failure data. The conceptual model presented here is a design-oriented model to provide the equipment designer with a means to understand the interrelationships between reliability, design and application variables.

CONCLUSIONS

Surface mount technology has emerged to optimize the high-density, high-speed integrated circuit performance of today's microelectronics. The mature manufacturing processes employed with conventional DIP componentry are taking a back seat to SMT, which is quickly becoming accepted industry-wide. By challenging the cost, size, weight and performance characteristics of previous manufacturing methods, surface-mounting is better meeting the demands and competitive pressures of advancing microcircuit miniaturization.

Upon initial analysis, a major stumbling block appears to be the large capital investment and total commitment needed to venture into SMT. Further investigations, however, indicate that the total life cycle costs will be substantially lower in the long run; consequently, those who falter in the decision to accept SMT may very well be left behind.

The failure mechanisms specific to surface mount technology revolve around the stresses which propagate into the solder connections. Modifications in everything from package lead designs to solder alloy compositions to substrate material and construction have been investigated to determine the most effective methods for alleviating this problem.

Reliability models are given to estimate the failure rates of surface mount packages, solder joint connections and printed wiring boards. It is recognized that the models presented are an initial step in a process which requires the incorporation of more extensive data and research.

The military is voicing reservations about the use of leadless ceramic chip carriers and has recently engaged in an investigation to evaluate the situation. A Tri-Service committee, The Ad Hoc Working

Group on Surface Mount Devices is actively assessing the potential risk of using leadless chip carrier technology in military systems currently being deployed and systems under design. The committee is considering restricting the use of leadless chip carriers in favor of leaded carriers in all future DoD applications.

REFERENCES

1. Reynolds, Robert A., "SMDs Invade Military and Commercial Equipment." Electronic Packaging and Production, February 1985, pg. 130.

2. Isaacson, Dale R., and Caswell, Gregory K., "Implementing Copper Thick Film Substrates for Surface Mounted Technology." Presented at the IPC Annual Meeting, April 1985, pg. 6.

3. Maerschalk, Joseph C., "Chip Carriers Today and Tomorrow." Journal of Electronic Defense, February 1986, pg. 51.

4. Shioleno, Lewis J., "Technology Takeoff Adds to Allure of Surface Mounting." Electronic Products, February 1, 1985, pg. 53.

5. Kneale, Dennis, "Improved Circuitry Technique Coming Into Its Own At Last." The Wall Street Journal, September 13, 1985, pg. 29.

6. Balde, John W., "Surface Mount Technology." ISHM Technical Monograph Series 6984-002, 1984, pg. 2.

7. Meehan, Robert, "The Package Can Make or Break a System's Performance." Electronic Packaging and Production, February 1985, pg. 146.

8. Walker, Mauro J., "Surface Mounted Device: Hybrid Module Technology Trade-offs in Communications Equipment." 1983 Proceedings of the International Microelectronics Symposium, pg. 28.

9. Fennimore, John E., "Using Leadless Components Technology on Printed Wiring Boards." Electronic Packaging and Production, December 1978, pg. 130.

10. Murray, Bruce, "Choosing the Right Surface Mount Adhesive." Machine Design, October 25, 1984, pg. 90.

REFERENCES (CONTINUED)

11. Knebusch, Mark, "Shrinking Circuit Boards with Surface Mount Components." Machine Design, May 24, 1984, pg. 73.

12. Fuqua, Norman B., "ESD Control in the Manufacturing Environment" (SOAR-6). IIT Research Institute, Summer 1986.

13. Institute for Interconnecting and Packaging Electronic Circuits, "Solderability Test Method for Printed Wiring Boards." IPC-S-804, 1980.

14. Tygard, Charles M, "Probes Ease Testing of Hybrids and SMT Assemblies." Electronic Packaging and Production, February 1986, pg. 205.

15. Conversation between Susan Stockman (IITRI) and Eugene Blackburn (RADC) at the RADC facility on 26 September 1985.

16. Caswell, Greg, "Vapor Phase Soldering of SMDs: Reliability Characteristics." Circuit World, 1985, pg. 17.

17. Winther, W.P., "Component Trends for Surface Mounting on Printed Circuit Boards." 1982 Proceedings of the National Electronic Packaging and Production Conference, pg. 312.

18. Triad Engineering Corporation, "Surface Mount Technology: A Quick Start Guide." October 1984, pp. 7-11.

19. Beedie, Mitch, "Surface Mount Packaging." Electronic Design, January 10, 1985, pg. 239.

20. Waller, D., Fox, L., and Hannemann, R., "Analysis of Surface Mount Thermal and Thermal Stress Performance." 1983 Proceedings of the 33rd Electronic Components Conference.

REFERENCES (CONTINUED)

21. Balde, John W., "VLSI Packages: Pin Grids or Chip Carriers." Circuits Manufacturing, September 1983, pg. 72.

22. Knausenberger, W.H., and Teneketges, N.A., "High Pinout IC Packaging and the Density Advantage of Surface Mounting." 1983 Proceedings of the IEEE Transactions on Components, Hybrids and Manufacturing Technology.

23. Wright, Robert W., "Polymer/Metal Substrates Minimize SMD Thermal Expansion Problems." Electronic Packaging and Production, February 1984, pg. 112.

24. Hagqe, John K., "Critical Component Requirements for Vapor Phase Soldering Leadless Components on Circuit Board Assemblies for Military Electronics." IEEE Transactions on Components, Hybrids and Manufacturing Technology, December 1983, pg. 445, 446.

25. DeVore, John A., "Fatigue Resistance of Solders." 1982 Proceedings of the National Electronic Packaging and Production Conference.

26. Panousis, N.T., and Kershner, R.C., "Solder Attachment of Leaded Components to Thick Film Hybrids." 1981 Proceedings of the IEEE Electronic Components Conference, pg. 165.

27. Hall, P.M., "Solder Attachment of Leadless Ceramic Chip Carriers." Solid State Technology, March 1983, pg. 105.

28. Brice-Heames, Kenneth, "Direct Attachment of Leadless Chip Carriers to Various PWB Material." 1984 Proceedings of the International Symposium on Microelectronics, pg. 479.

29. Engelmaier, Werner, "Functional Cycles and Surface Mounting Attachment Reliability." Surface Mount Technology: ISHM Technical Monograph Series 6984-002, 1984, pg. 102.

REFERENCES (CONTINUED)

30. Hall, P.M., and Morabito, J.M., "Recent Advances in Solder Bond Technology for Microelectronic Packaging." 1980 International Conference on Metallurgical Coatings, pg. 436.

31. Chappell, Charles D., and Banas, Edward C., "Integrating Surface Mounted Technology Into Manufacturing." 1984 Proceedings of the 34th Electronic Components Conference, pg. 516.

32. Howard, Robert T, Sobeck, Steven W., and Sanetra, Christopher, "A New Package-Related Failure Mechanism for Leadless Ceramic Chip Carriers (LC-3s) Solder-Attached to Alumina Substrates." Solid State Technology, February 1983, pg. 118.

33. Roos-Kozel, Barbara, "Solder Pastes." Surface Mount Technology: ISHM Technical Monograph Series 6984-002, 1984, pp. 118, 119.

34. Gray, Foster, "Substrates for Chip Carrier Interconnections." Surface Mount Technology: ISHM Technical Monograph Series 6984-002, 1984.

35. Coit, David W., "Printed Wiring Assembly and Interconnection Reliability." RADC-TR-81-318, November 1981.

36. Harley, Strong and Young, "Reliability Investigation of Thermal Stress/Fatigue Failure in Multilayer Interconnection Board." RADC-TR-70-192, 1970.

37. Mahar, David, and Rossi, Michael, "Microcircuit Device Reliability: Field Experience Data Base" (MDR-21A). IIT Research Institute, Spring 1985.

38. Rossi, Michael, "Nonelectronic Parts Reliability Data" (NPRD-3). IIT Research Institute, Fall 1985.

REFERENCES (CONTINUED)

39. Chen, C.H., and Verville, J.M., "Direct Mounting of Ceramic Leadless Chip Carrier Onto Glass Epoxy Circuit Board." 1983 Proceedings of the International Microelectronics Symposium, pg. 25.

40. Timmis, David L., "An Elastomeric Interconnection System for Fine Pitch Leadless Chip Carriers." 1984 Proceedings of the 34th Electronic Components Conference, pg. 141.

41. Greer, W.T., "Post Molded Leaded Chip Carrier." Texas Instruments, 1983, pg. 3.

42. Manson, S.S., "Thermal Stress and Low Cycle Fatigue." McGraw-Hill, 1966.

43. Brodsky, Parker and Stafford, "Reliability and Application of Leaded Plastic Chip Carriers." Electronic Packaging and Production, November 1981.

44. Smeby, "Solder Joint Behavior in HCC/PWP Interconnects." 1984 Proceedings of the 34th Electronic Components Conference.

45. Riemer and Russell, "The Optimized Solder Bond for Ceramic Chip Carriers on Ceramic Boards." 1983 Proceedings of the International Symposium on Microelectronics.

46. Wright, Edgar A., "Thermal Shock Testing of Ceramic Thick Film Substrates." 1984 Proceedings of the International Symposium on Microelectronics, pg. 43.

47. Martin, Jacob H., and Hanley, David, "Humidity Test of Premolded Chip Carriers." 1980 Proceedings of the 30th Electronic Components Conference.

REFERENCES (CONTINUED)

48. Danielson, Hans, "Chip Carriers on Ceramic Thick Film Multilayer Boards In High Reliability Applications." 1984 Proceedings of the International Symposium on Microelectronics.

49. Wright, Edgar A. and Wolverton, W. Michael , "The Effect of the Solder Reflow Method and Joint Design on the Thermal Fatigue Life of Leadless Chip Carrier Solder Joints." 1984 Proceedings of the 34th Electronic Components Conference, pg. 153.

50. Flodman, G., "An Unsymmetric Metal Base PWB: Design Parameters and Thermal Considerations." Circuit World, 1985, pg. 27.

51. Williams, J.A., "Derivation of a Failure Law for Creep Under Cyclic Stress." Fatigue at Elevated Temperatures, ASTM STP 520, American Society for Testing and Materials, 1973.

52. Takenaka, T., Kobayashi, F., Nestu, T. and Imada H., "Reliability of Flip-Chip Interconnections." 1984 Proceedings of the International Microelectronics Symposium.

53. Clatterbaugh, G.V., and Charles, H.K., Jr., "Thermomechanical Behavior of Soldered Interconnects for Surface Mounting: A Comparison of Theory and Experiment." The Johns Hopkins University Applied Physics Laboratory.

54. Engelmaier, Werner, "Effects of Power Cycling on Leadless Chip Carrier Mounting Reliability and Technology." Electronic Packaging and Production, April 1983.

55. Dey, K.A., "Practical Statistical Analysis for the Reliability Engineer" (SOAR-2). IIT Research Institute, Spring 1983.

REFERENCES (CONTINUED)

56. Hall, P.M., "Solder Post Attachment of Ceramic Chip Carriers to Ceramic Film Integrated Circuits." 1981 Proceedings of the 31st Electronic Components Conference, pg. 176.

57. Lanti, Delany and Hines, "The Characteristic Wearout Process in Epoxy-Glass Printed Wiring Circuits for High Density Electronic Packaging." Bell Laboratories.

APPENDIX A:

SMT FAILURE EVENT DATA

Appendix A includes SMT failure event data for microcircuits. Presented first are the data tables. Following the data tables are graphical depictions of the data in pie chart form.

This first section of Appendix A contains failure event data tables. The tables provide quantitative information about the frequency of failure indicators and failure locations. For the purposes of this text these were defined as:

(1) A failure indicator is the first externally detectable effect of a part failure.

(2) A failure location is the physical location of a defect or failure within a device.

The data (when available) are presented in a number of different tables. These tables break down the data into six functional groups,

- Digital SSI/MSI (< 100 gates)
- Linear
- Interface
- Memory (<16k bits)
- Digital LSI (>100 gates but < 500 gates)
- VLSI (>500 gates or > 16k bits of Memory)

and package construction. Only Flat Pack (FP) and Chip Carrier (CC) in Hermetic and Nonhermetic packages are reported.

The tables consist of five columns:

- The first column describes the "failure indicator" or "failure location" in descriptive terms relative to three levels of detail.

- The second column contains the total number of test "lots" that were available for that indicator or location.

- The third column contains the total number of "failures" that were available from the lots for a given indicator or location.

- The forth column indicates the total "time of operation" for all of the lots of a given indicator or location.

- The fifth column provides the "Average Time to Detection (AVG/TTD)" of devices that have failed. This is the summation of the failure times divided by total failures for a given indicator or location.

The microcircuit failure event distributions represent data compiled from a variety of data sources such as life test, screening and field. They are therefore subject to constraints associated with variances in the content of each failure analysis report. The summarized results are dependent on the quality of data supplied and the extent to which the failure analyses were performed. If the unknown failure indicators or modes are distributed similarly to those which are known, then these percentages represent the actual failure indicator or failure mode percentages.

The use of these tables, particularly the failure indicator tables, will be beneficial to reliability engineers performing Failure Mode Effects and Criticality Analysis (FMECA) in the evaluation of system designs.

Failure Event (Failure Indicator) Digital SSI/MSI,Hermetic,Flat Pack

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Open	Verified Open	Unknown	20	40	200	40.4000
Open	Verified Open	Input	5	5	0	.0000
Open	Verified Open	Output	2	2	0	.0000
Open	Verified Open	Supply	3	5	128	76.8000
Open	Verified Open	Other	1	1	0	.0000
Open	Intermittent Open	Unknown	2	2	0	.0000
Short	Verified Short	Unknown	21	26	0	.0000
Short	Verified Short	Input	9	9	0	.0000
Short	Verified Short	Output	2	2	0	.0000
Short	Verified Short	Combination	11	11	128	11.6363
Short	Verified Short	Other	1	2	0	.0000
Short	Intermittent Short	Unknown	1	1	0	.0000
Short	Intermittent Short	Input	1	1	0	.0000
Short	Intermittent Short	Combination	2	2	0	.0000
Degraded			18	22	0	.0000
Leakage	Unknown		6	6	0	.0000
Leakage	Input		6	8	0	.0000
Leakage	Supply		2	2	96	48.0000
Leakage	Combination		6	6	512	85.3333
Parameter Tolerance	Output Voltage		1	1	0	.0000
Parameter Tolerance	Input Voltage		1	1	1,000	1000.0000
Parameter Tolerance	Switching Characteristics		5	5	0	.0000
Parameter Tolerance	Supply Current		2	2	0	.0000
Parameter Tolerance	Input Offset Current		1	3	0	.0000
Parameter Tolerance	Dynamic Characteristics		1	1	0	.0000
Parameter Tolerance	Low Level Output Current		1	1	0	.0000
Parameter Tolerance	High Level Input Current		1	1	0	.0000
Parameter Tolerance	Combination		1	1	0	.0000
Functional Anomaly	Unknown		17	2,689	0	.0000

Failure Event (Failure Indicator) Digital SSI/MSI,Hermetic,Flat Pack

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Functional Anomaly	Inoperative, Catastrophic		6	6	0	.0000
Functional Anomaly	Improper Output	Unknown	1	1	0	.0000
Functional Anomaly	Improper Output	Improper Logic State	4	4	0	.0000
Functional Anomaly	Improper Output	Improper Output Switching	1	2	0	.0000
Functional Anomaly	Improper Output	Fluctuating,Oscill Output	1	1	0	.0000
Functional Anomaly	Improper Output	Distorted, Clipped Output	1	1	0	.0000
Functional Anomaly	Output Latching	Latched High	5	5	0	.0000
Functional Anomaly	Output Latching	Latched Low	1	1	0	.0000
Mechanical Anomaly			38	645	1,336	2.0713

Failure Event (Failure Indicator) Digital SSI/MSI,Hermetic,Chip Carrier

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Short	Verified Short	Unknown	1	30	0	.0000
Mechanical Anomaly			1	1	0	.0000

Failure Event (Failure Indicator) Linear,Hermetic,Flat Pack

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Open	Verified Open	Unknown	3	3	0	.0000
Open	Verified Open	Input	2	2	0	.0000
Open	Verified Open	Combination	1	1	0	.0000
Short	Verified Short	Unknown	5	6	24	4.0000
Short	Verified Short	Input	1	2	0	.0000
Short	Verified Short	Output	1	1	0	.0000
Short	Verified Short	Supply	2	2	0	.0000
Short	Verified Short	Combination	2	9	0	.0000
Short	Intermittent Short	Other	1	1	0	.0000
Degraded			5	6	0	.0000
Leakage	Unknown		4	6	0	.0000
Leakage	Output		1	1	0	.0000
Parameter Tolerance	Unknown		2	3	0	.0000
Parameter Tolerance	Input Offset Voltage		1	1	0	.0000
Parameter Tolerance	Switching Characteristics		1	1	0	.0000
Parameter Tolerance	Gain Characteristics		3	4	0	.0000
Functional Anomaly	Unknown		3	4	0	.0000
Functional Anomaly	Inoperative, Catastrophic		15	31	16	.5161
Functional Anomaly	Improper Output	Unknown	3	3	0	.0000
Functional Anomaly	Output Latching	Unknown	1	1	0	.0000
Functional Anomaly	Output Latching	Latched High	2	2	0	.0000
Functional Anomaly	Output Latching	Latched Low	1	1	0	.0000
Mechanical Anomaly			12	16	6	.3750

Failure Event (Failure Indicator) Linear,Hermetic,Chip Carrier

FAILURE INDICATOR		LOTS	FAILS	TIME	AVG/TTD
Functional Anomaly	Unknown	1	2	0	.0000
Mechanical Anomaly		1	2	0	.0000

Failure Event (Failure Indicator) Interface,Hermetic,Flat Pack

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Open	Verified Open	Supply	2	5	0	.0000
Degraded			4	5	0	.0000
Leakage	Unknown		1	2	0	.0000
Leakage	Input		2	2	0	.0000
Parameter Tolerance	Unknown		1	3	0	.0000
Parameter Tolerance	Switching Characteristics		2	2	0	.0000
Functional Anomaly	Unknown		2	4	0	.0000
Functional Anomaly	Inoperative, Catastrophic		4	19	0	.0000
Functional Anomaly	Improper Output	Unknown	3	2	0	.0000
Functional Anomaly	Improper Output	Fluctuating,Oscill Output	1	1	0	.0000
Functional Anomaly	Output Latching	Unknown	1	1	0	.0000
Functional Anomaly	Output Latching	Latched High	1	1	0	.0000

Failure Event (Failure Indicator) Interface,Hermetic,Chip Carrier

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Short	Verified Short	Unknown	1	1	0	.0000
Mechanical Anomaly			1	3	0	.0000

Failure Event (Failure Indicator) Memory,Hermetic,Flat Pack

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Short	Verified Short	Combination	1	13	0	.0000
Functional Anomaly	Unknown		1	1	168	168.0000
Functional Anomaly	Improper Output	Unknown	1	1	0	.0000
Functional Anomaly	Output Latching	Latched High	2	2	0	.0000

Failure Event (Failure Indicator) Memory,Hermetic,Chip Carrier

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Short	Verified Short	Unknown	1	2	0	.0000
Functional Anomaly	Unknown		1	8	0	.0000
Mechanical Anomaly			1	2	0	.0000

Failure Event (Failure Indicator) Digital LSI,Hermetic,Flat Pack

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Open	Verified Open	Unknown	1	1	0	.0000
Open	Verified Open	Input	1	1	3,060	3060.0000
Open	Verified Open	Other	1	1	4,346	4346.0000
Short	Verified Short	Unknown	1	1	0	.0000
Short	Verified Short	Output	1	1	4,010	4010.0000
Degraded			12	24	37,987	3629.7916
Leakage	Unknown		1	1	2,000	2000.0000
Functional Anomaly	Unknown		2	3	0	.0000
Functional Anomaly	Inoperative, Catastrophic		1	3	0	.0000

Failure Event (Failure Indicator) VLSI,Hermetic,Flat Pack

FAILURE INDICATOR		LOTS	FAILS	TIME	AVG/TTD
Functional Anomaly	Unknown	1	2	1,000	1000.0000

Failure Event (Failure Indicator) VLSI,Non Hermetic,Chip Carrier

FAILURE INDICATOR		LOTS	FAILS	TIME	AVG/TTD
Functional Anomaly	Unknown	5	5	502	100.4000

Failure Event (Failure Indicator) VLSI,Non Hermetic,Chip Carrier

FAILURE INDICATOR	LOTS	FAILS	TIME	AVG/TTD
Mechanical Anomaly	1	1	0	.0000

Failure Event (Failure Indicator) VLSI,Hermetic,Chip Carrier

FAILURE INDICATOR			LOTS	FAILS	TIME	AVG/TTD
Open	Verified Open	Unknown	3	3	0	.0000
Parameter Tolerance	Unknown		4	14	3,160	765.7142
Parameter Tolerance	Output Voltage		2	3	2,000	1000.0000
Parameter Tolerance	Combination		1	4	1,080	1080.0000

Failure Event (Failure Location) Digital SSI/MSI,Hermetic,Flat Pack

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Die	Unknown		20	28	480	17.1428
Die	Bulk Aspects	Unknown	1	6	0	.0000
Die	Bulk Aspects	Junction	6	8	0	.0000
Die	Bulk Aspects	Diffusion	1	1	0	.0000
Die	Metalization	Unknown	39	48	128	8.0000
Die	Metalization	Contact Window	11	11	0	.0000
Die	Oxide/Dielectric	Unknown	6	7	1,296	185.1428
Die	Oxide/Dielectric	Gate Oxide/Dielectric	9	14	0	.0000
Die	Oxide/Dielectric	Field Oxide/Dielectric	1	1	0	.0000
Die	Glassivation/Overcoat		3	4	0	.0000
Die	Surface		3	5	0	.0000
Interconnects	Wire		14	21	0	.0000
Interconnects	Wirebond	Unknown	5	6	128	21.3333
Interconnects	Wirebond	Wirebond at D.P. Unknown	7	43	0	.0000
Interconnects	Wirebond	Wirebond at L.F. Unknown	1	1	0	.0000
Package	Unknown		9	32	0	.0000
Package	Package Seal		12	36	0	.0000
Package	Package Seal	Leaky	5	6	0	.0000
Package	Package Lid		2	3	0	.0000
Package	Package Body		1	1	0	.0000
Package	Lead Frame/External Leads		21	28	0	.0000
Package	Die Attach Bond		5	5	0	.0000

Failure Event (Failure Location) Digital SSI/MSI,Hermetic,Chip Carrier

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Interconnects	Wire		1	30	0	.0000
Package	Package Seal	Leaky	1	1	0	.0000

Failure Event (Failure Location) Linear,Hermetic,Flat Pack

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Die	Unknown		4	6	0	.0000
Die	Bulk Aspects	Unknown	4	4	0	.0000
Die	Metalization	Unknown	13	27	0	.0000
Die	Metalization	Bond Pad	1	1	0	.0000
Die	Oxide/Dielectric	Unknown	1	1	0	.0000
Die	Oxide/Dielectric	Gate Oxide/Dielectric	4	5	0	.0000
Die	Glassivation/Overcoat		3	4	0	.0000
Die	Surface		2	2	0	.0000
Interconnects	Unknown		3	3	0	.0000
Interconnects	Wire		4	4	0	.0000
Interconnects	Wirebond	Unknown	6	10	0	.0000
Interconnects	Wirebond	Wirebond at D.P. Unknown	1	1	0	.0000
Interconnects	Wirebond	Wirebond at L.F. Unknown	1	1	0	.0000
Package	Unknown		3	3	6	2.0000
Package	Package Seal		1	1	0	.0000
Package	Package Body		1	1	0	.0000
Package	Lead Frame/External Leads		1	1	0	.0000
Package	Die Attach Bond		1	1	0	.0000

Failure Event (Failure Location) Linear,Hermetic,Chip Carrier

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Package	Package Seal	Leaky	1	2	0	.0000

Failure Event (Failure Location) Interface,Hermetic,Flat Pack

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Die	Unknown		2	3	0	.0000
Die	Bulk Aspects	Unknown	1	1	0	.0000
Die	Metalization	Unknown	2	7	0	.0000
Die	Oxide/Dielectric	Gate Oxide/Dielectric	5	16	0	.0000
Die	Surface		4	4	0	.0000
Interconnects	Wire		2	5	0	.0000
Package	Unknown		1	0	0	.0000
Package	Lead Frame/External Leads		1	3	0	.0000
Package	Die Attach Bond		2	4	0	.0000

Failure Event (Failure Location) Interface,Hermetic,Chip Carrier

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Interconnects	Wire		1	1	0	.0000
Package	Package Seal	Leaky	1	3	0	.0000

Failure Event (Failure Location) Memory,Hermetic,Flat Pack

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Die	Metalization	Unknown	1	1	0	.0000
Interconnects	Wirebond	Wirebond at D.P. Unknown	1	13	0	.0000
Interconnects	Wirebond	Wirebond at L.F. Unknown	2	1	0	.0000
Package	Lead Frame/External Leads		1	1	200	200.0000

Failure Event (Failure Location) Memory,Hermetic,Chip Carrier

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Package	Package Seal	Leaky	1	2	0	.0000
Package	Die Attach Bond		2	10	0	.0000

Failure Event (Failure Location) Digital LSI,Hermetic,Flat Pack

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Die	Bulk Aspects	Junction	3	3	2,000	666.6666
Die	Metalization	Unknown	3	7	0	.0000
Interconnects	Wirebond	Unknown	1	1	4,346	4346.0000
Package	Package Body		1	0	0	.0000

Failure Event (Failure Location) VLSI,Non Hermetic,Flat Pack

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Die	Surface		2	3	2,000	1000.0000

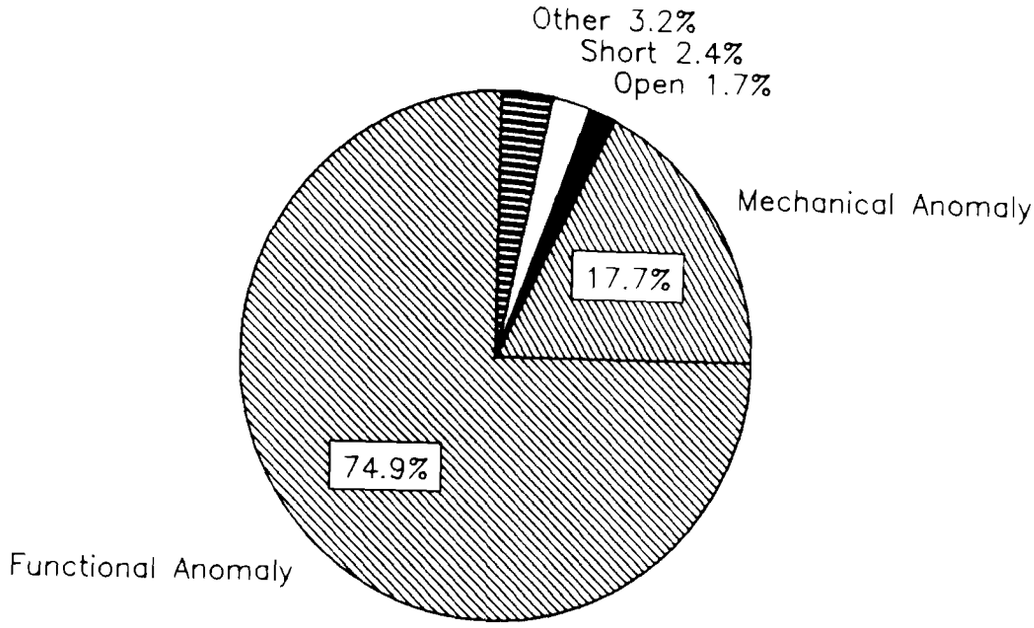
Failure Event (Failure Location) VLSI,Non Hermetic,Chip Carrier

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Interconnects	Wirebond	Unknown	3	3	214	71.3333
Package	Unknown		1	1	0	.0000

Failure Event (Failure Location) VLSI,Hermetic,Chip Carrier

FAILURE LOCATION			LOTS	FAILS	TIME	AVG/TTD
Interconnects	Wirebond	Wirebond at D.P. Unknown	3	3	0	.0000

Hermetic Flatpack



Hermetic Chip Carrier

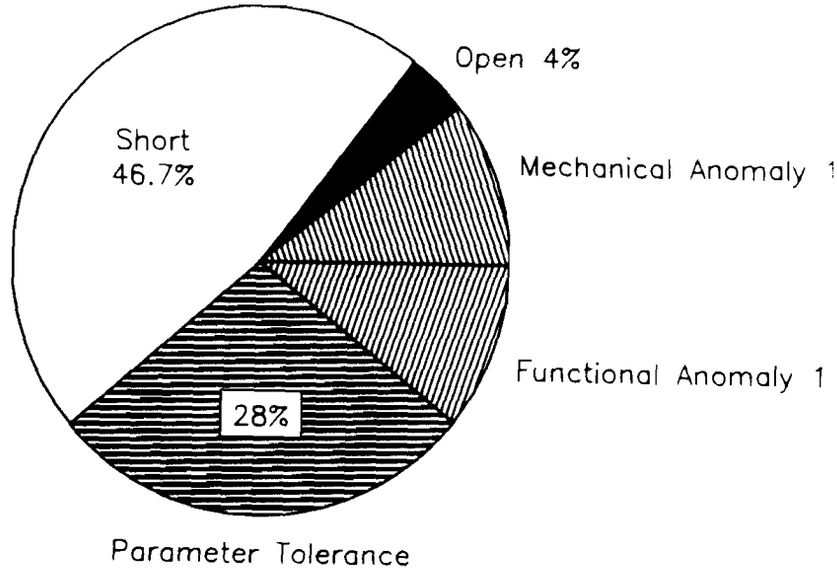


FIGURE A-1:

FAILURE INDICATOR
DEVICES FROM ALL FUNCTIONAL
GROUPS

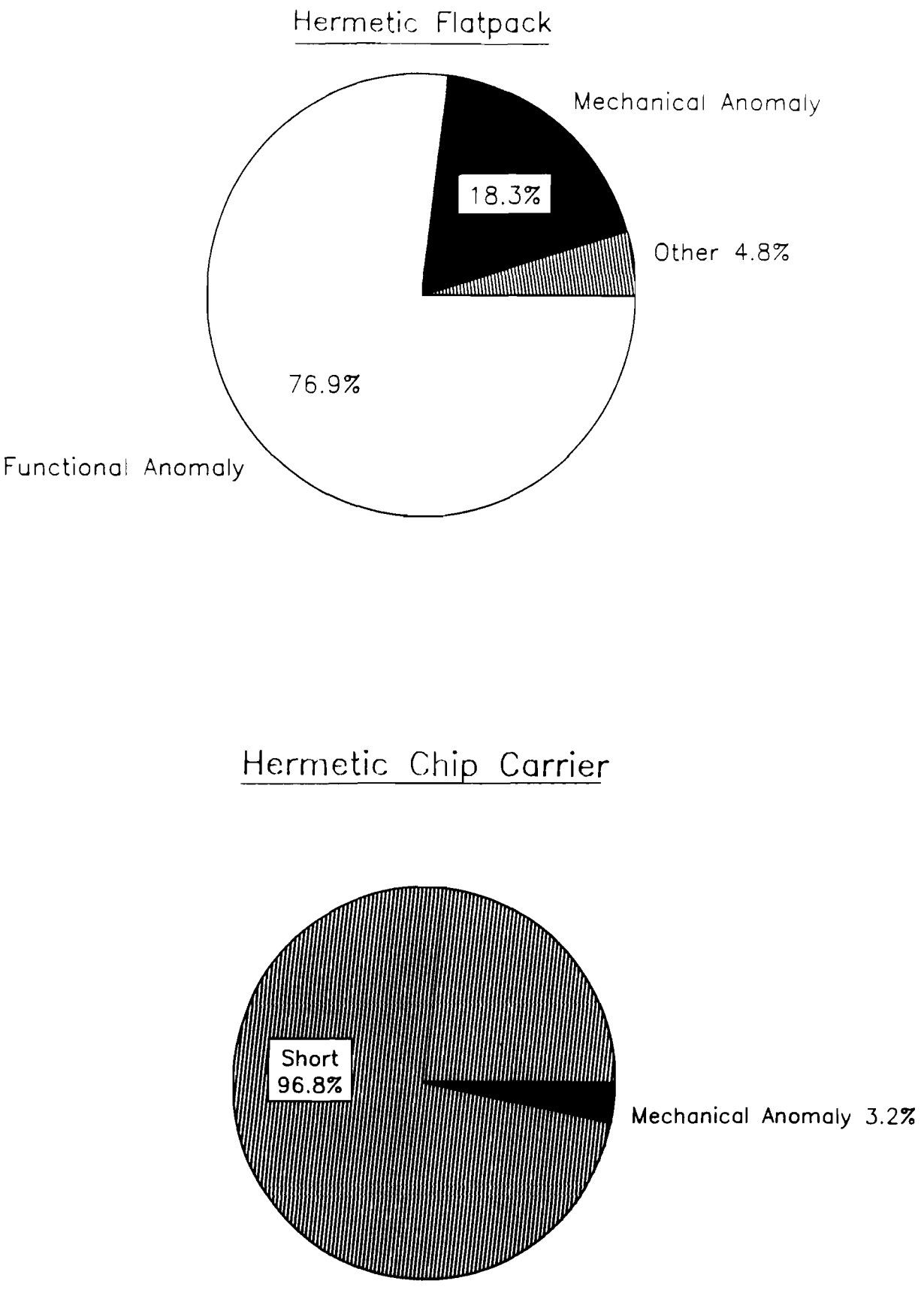
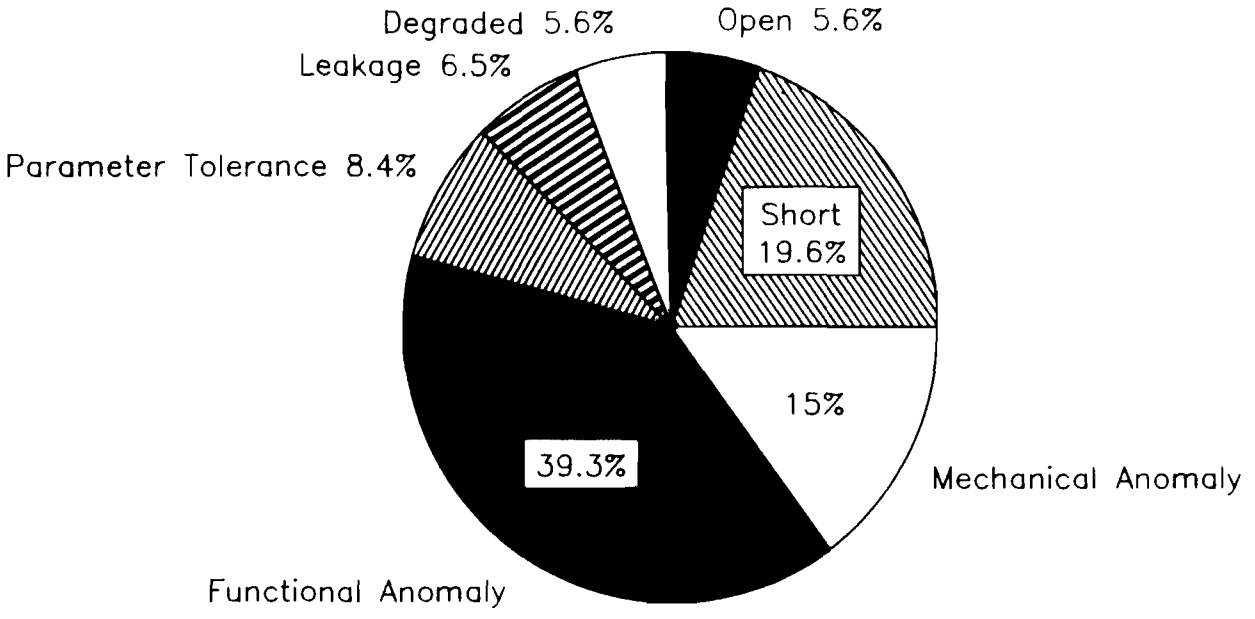


FIGURE A-2:

FAILURE INDICATOR

DIGITAL SSI/MSI DEVICES

Hermetic Flatpack



Hermetic Chip Carrier

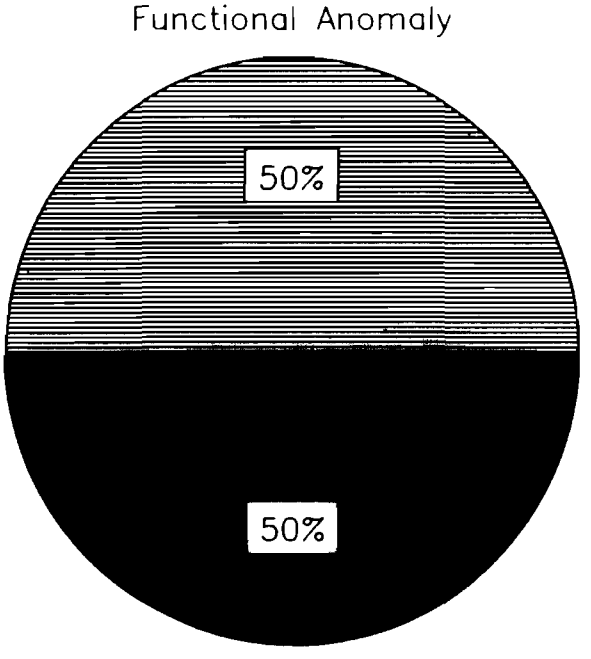
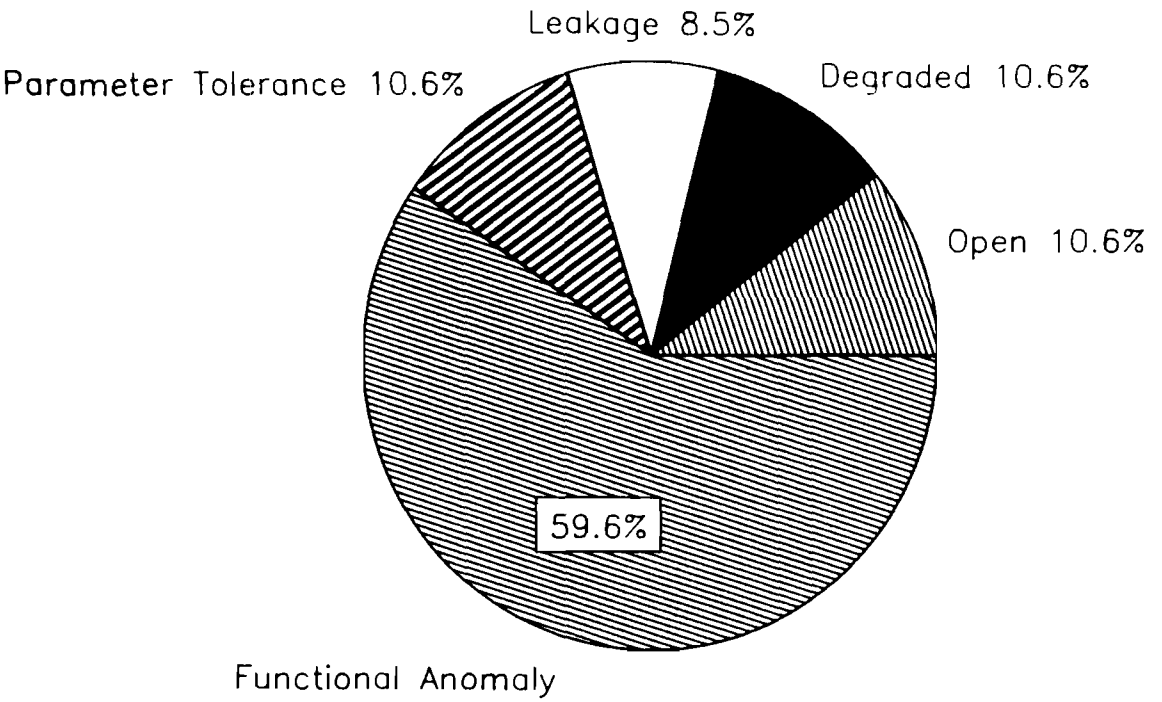


FIGURE A-3:

FAILURE INDICATOR
LINEAR DEVICES

Hermetic Flatpack



Hermetic Chip Carrier

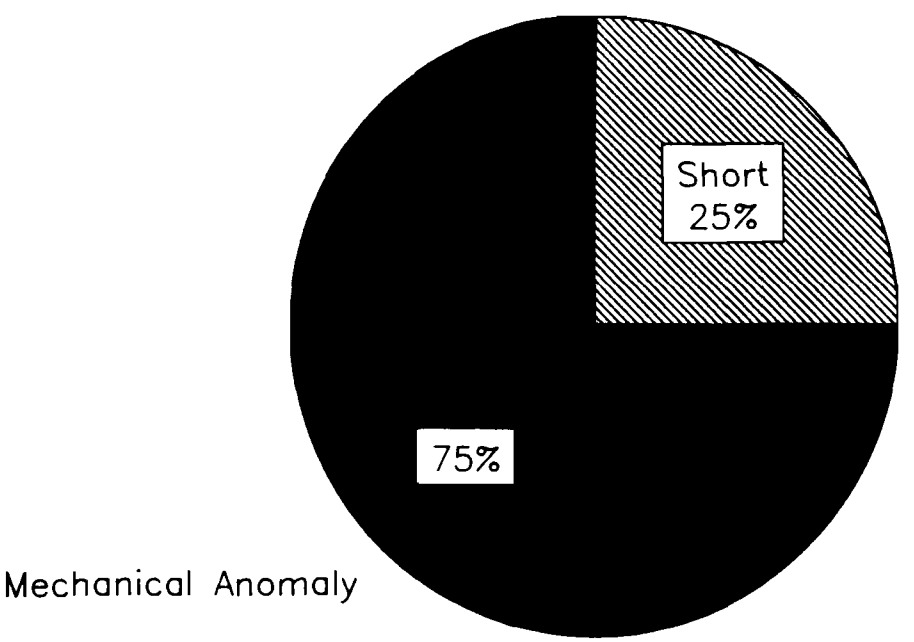
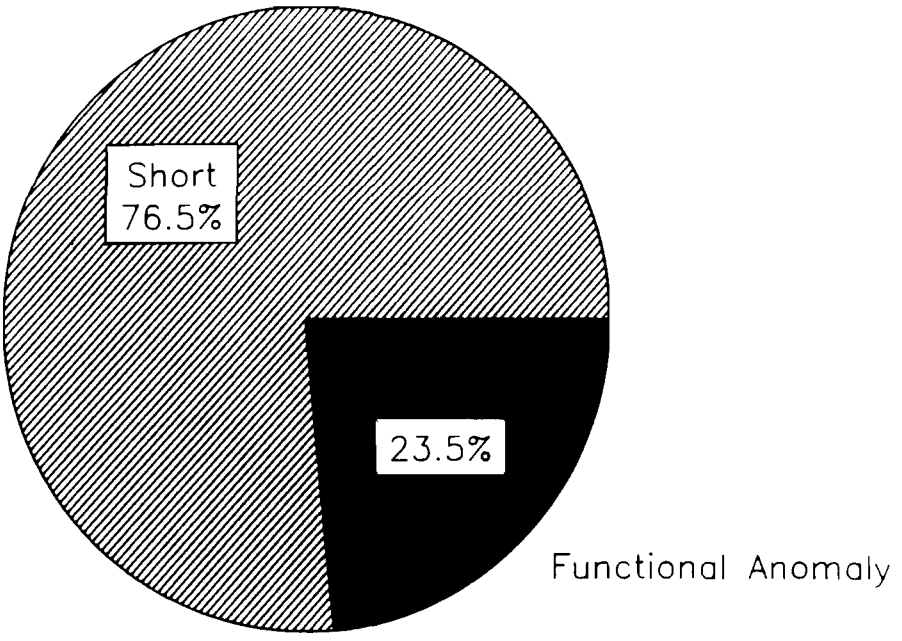


FIGURE A-4:
FAILURE INDICATOR
INTERFACE DEVICES

Hermetic Flatpack



Hermetic Chip Carrier

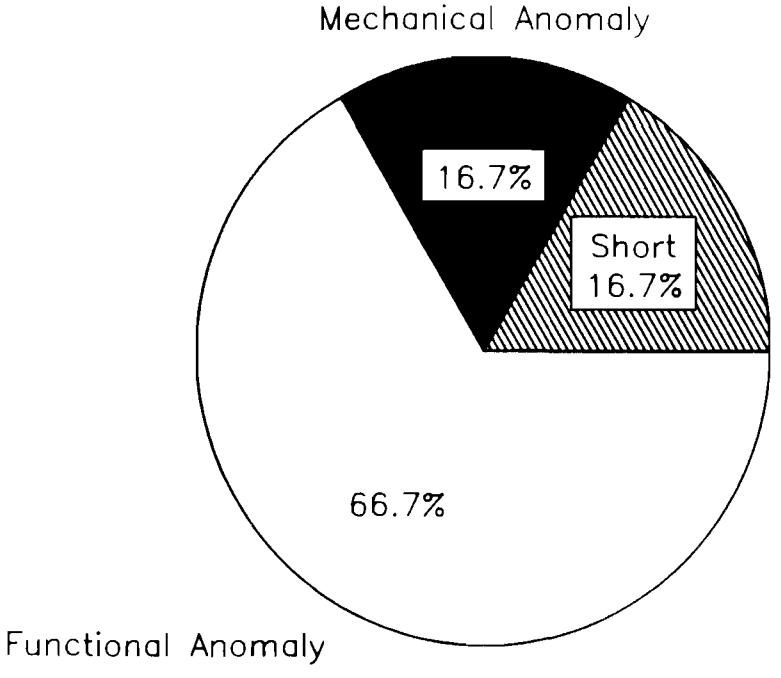


FIGURE A-5:

FAILURE INDICATOR
MEMORY DEVICES

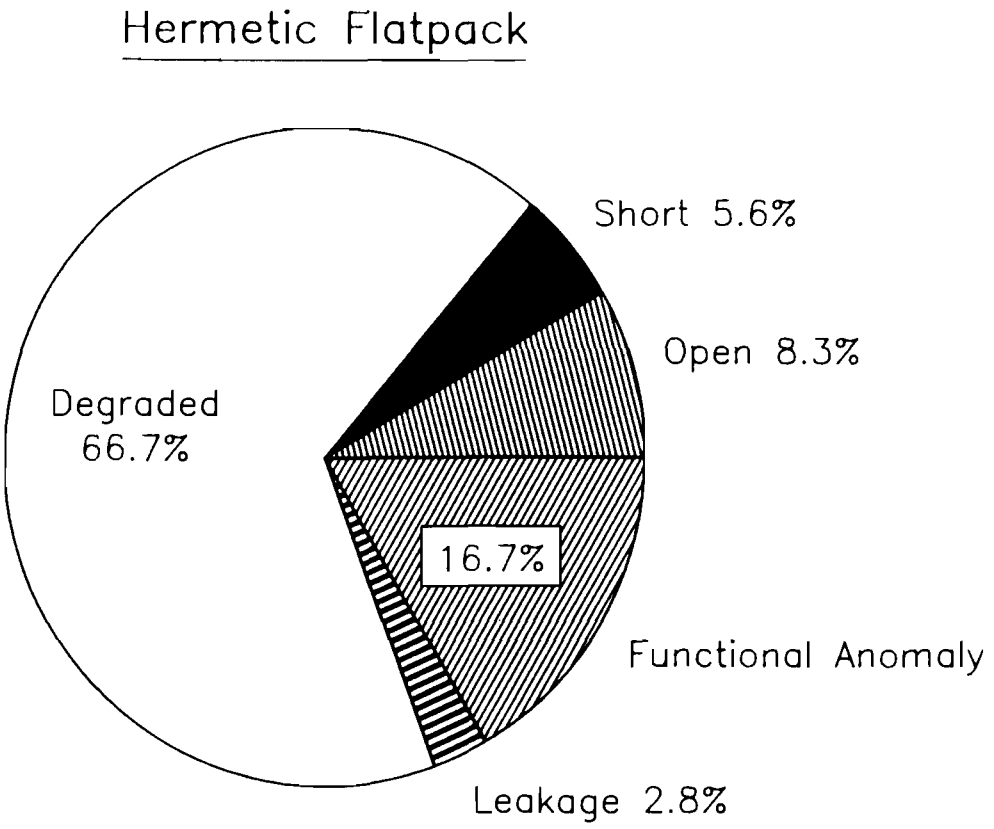
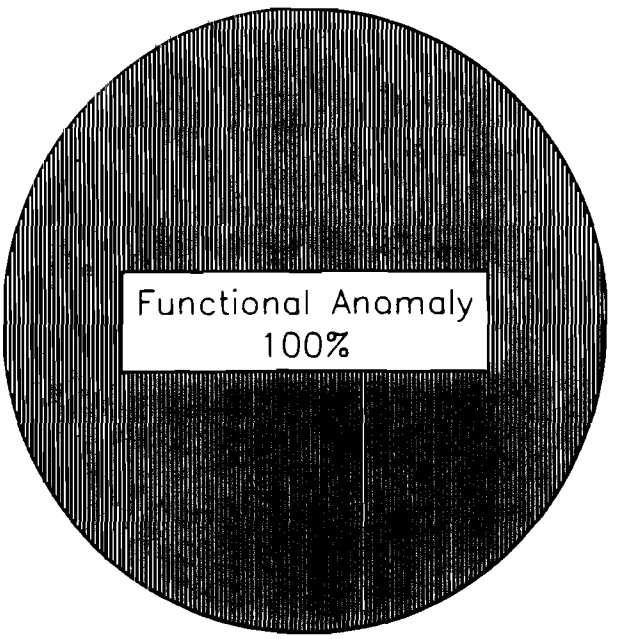


FIGURE A-6:
FAILURE INDICATOR
DIGITAL LSI DEVICES

Hermetic Flatpack



Hermetic Chip Carrier

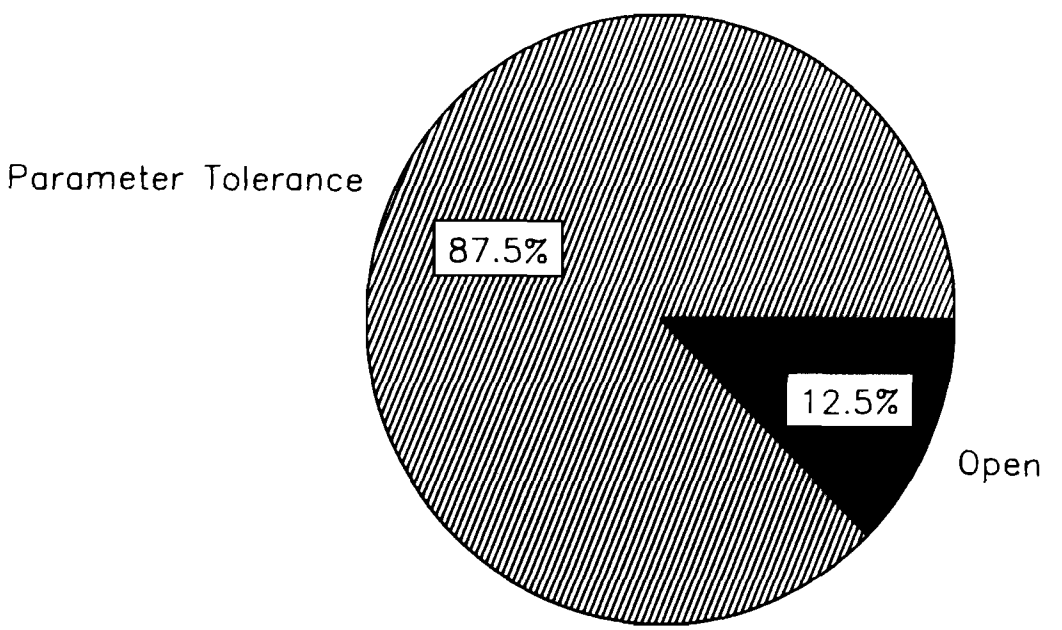


FIGURE A-7:
FAILURE INDICATOR
VLSI DEVICES

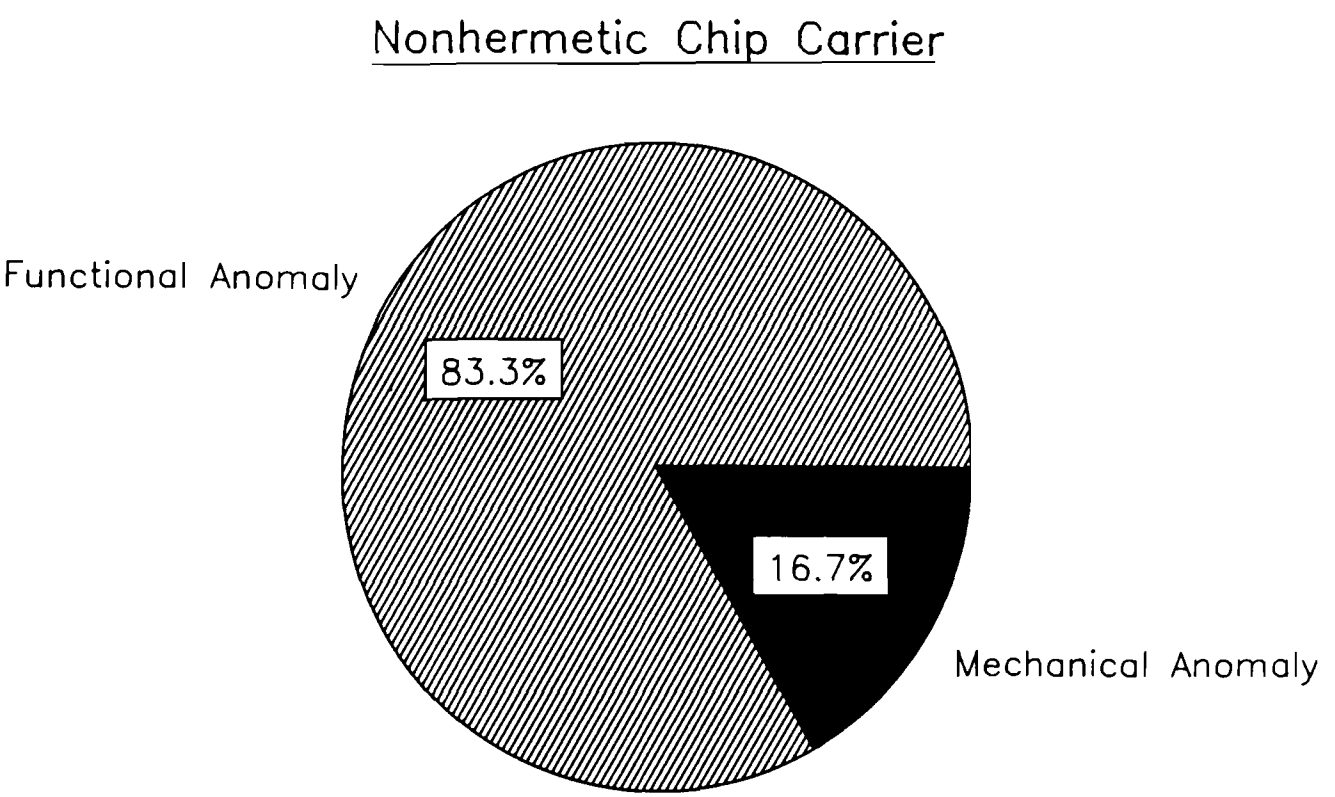
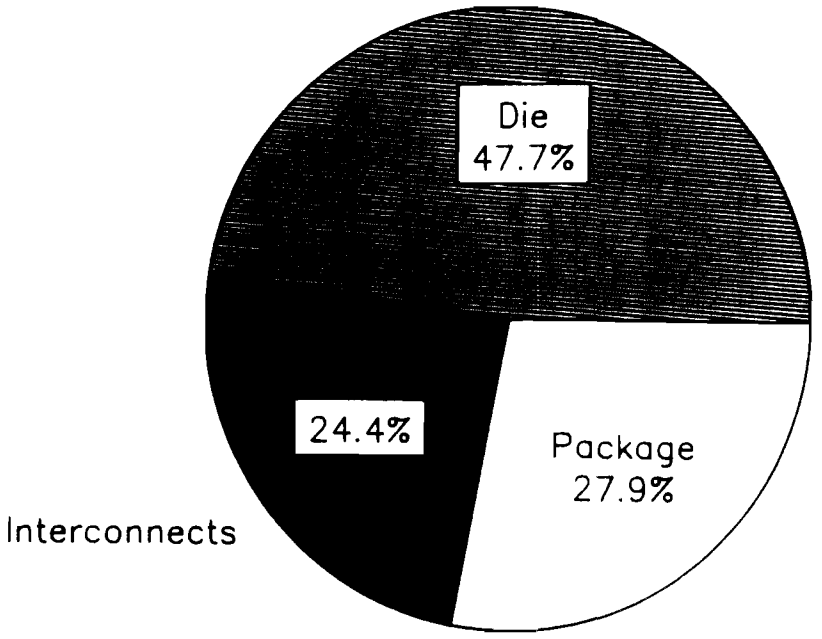


FIGURE A-8:
FAILURE INDICATOR
VLSI DEVICES

Hermetic Flatpack



Hermetic Chip Carrier

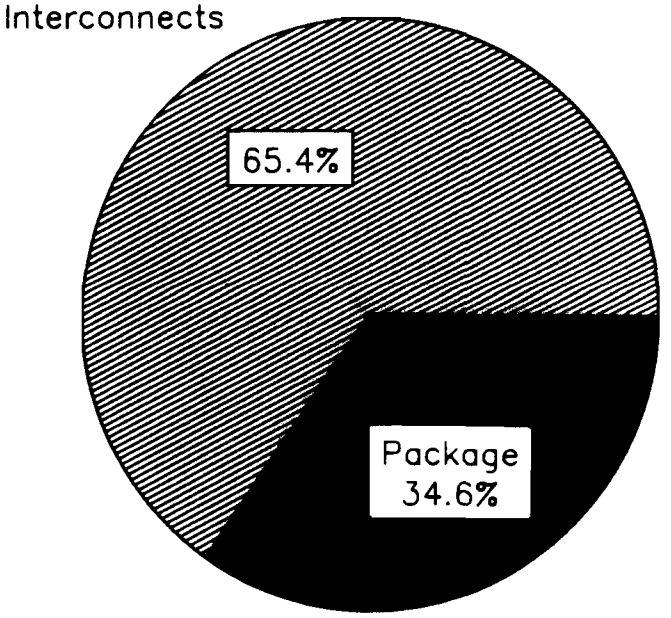
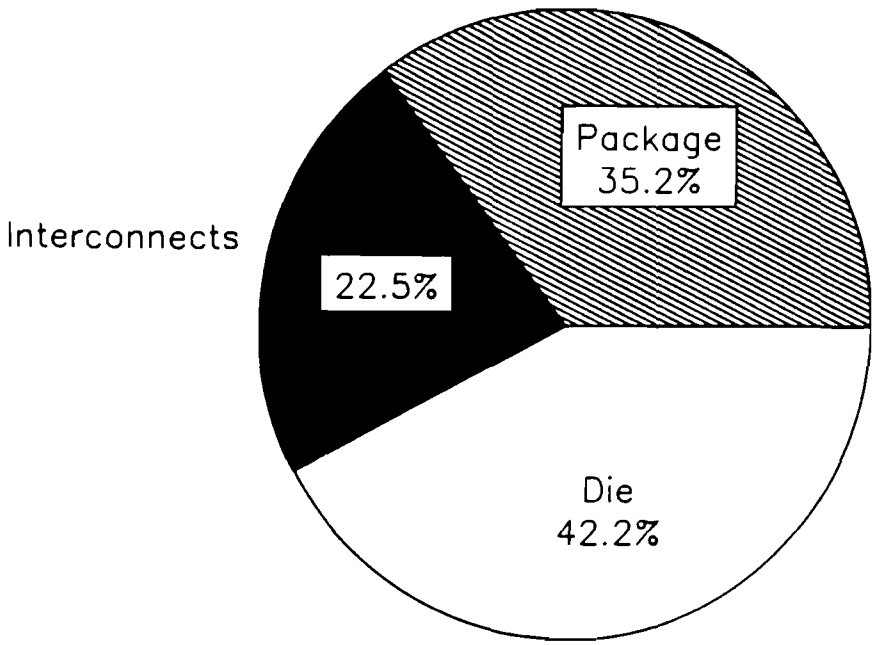


FIGURE A-9:
FAILURE LOCATION
DEVICES FROM ALL FUNCTIONAL
GROUPS

Hermetic Flatpack



Hermetic Chip Carrier

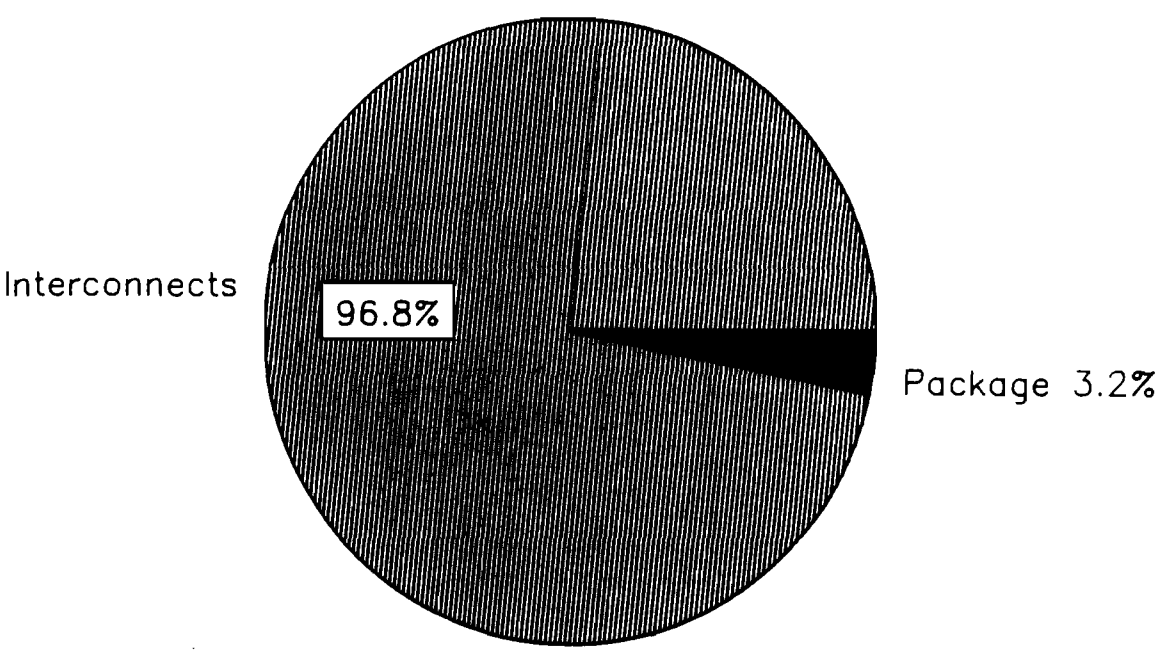
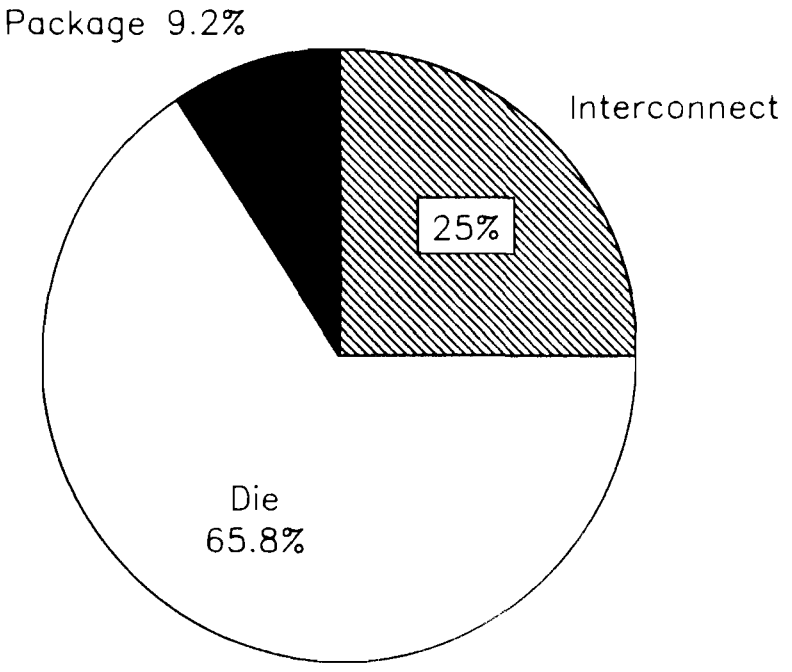


FIGURE A-10:
FAILURE LOCATION
DIGITAL SSI/MSI DEVICES

Hermetic Flatpack



Hermetic Chip Carrier

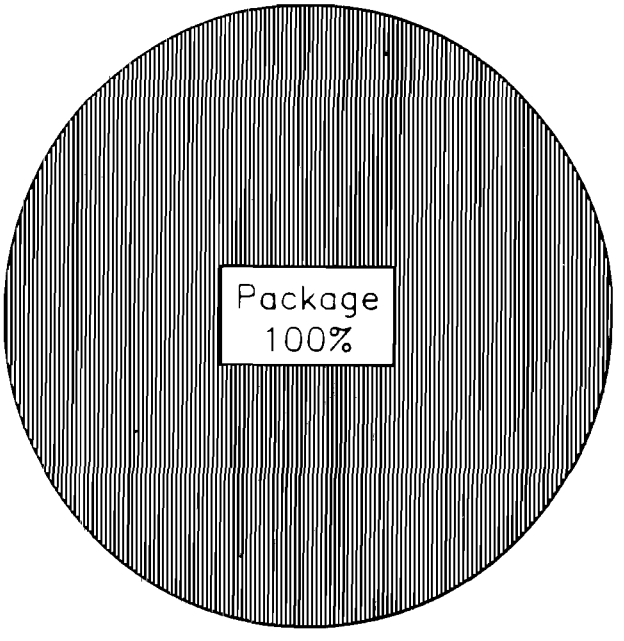
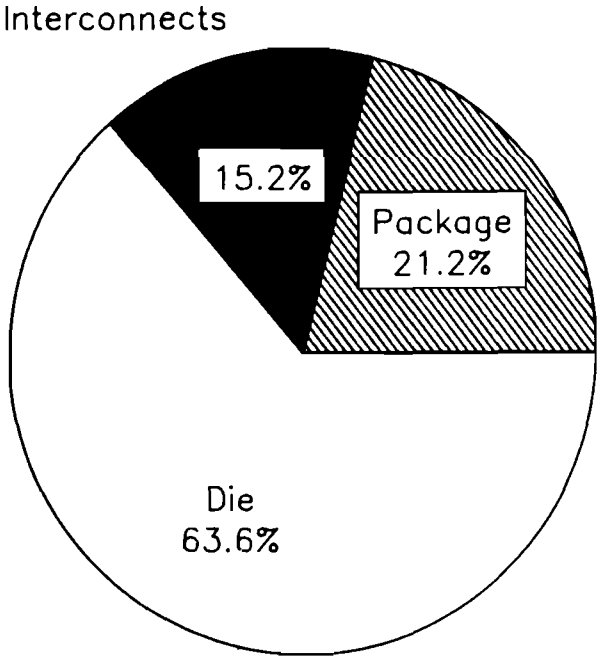


FIGURE A-11:
FAILURE LOCATION
LINEAR DEVICES

Hermetic Flatpack



Hermetic Chip Carrier

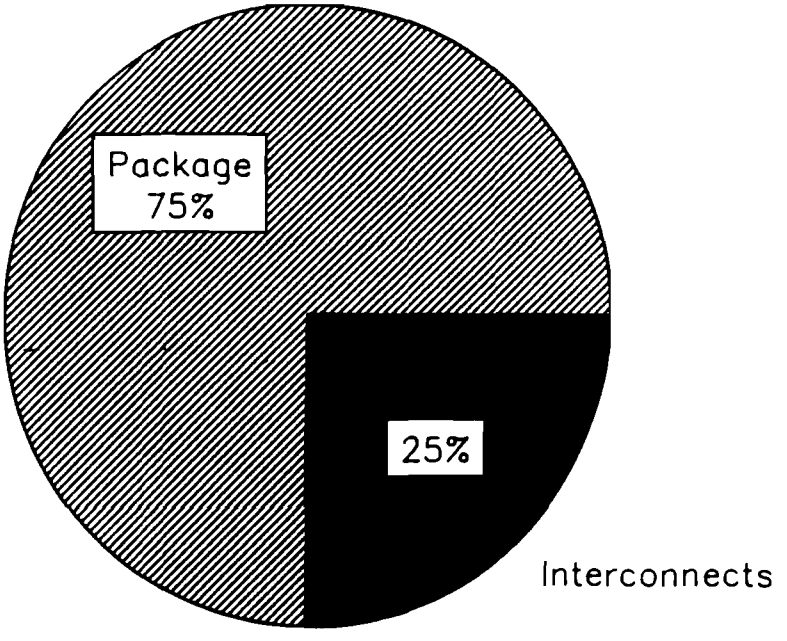
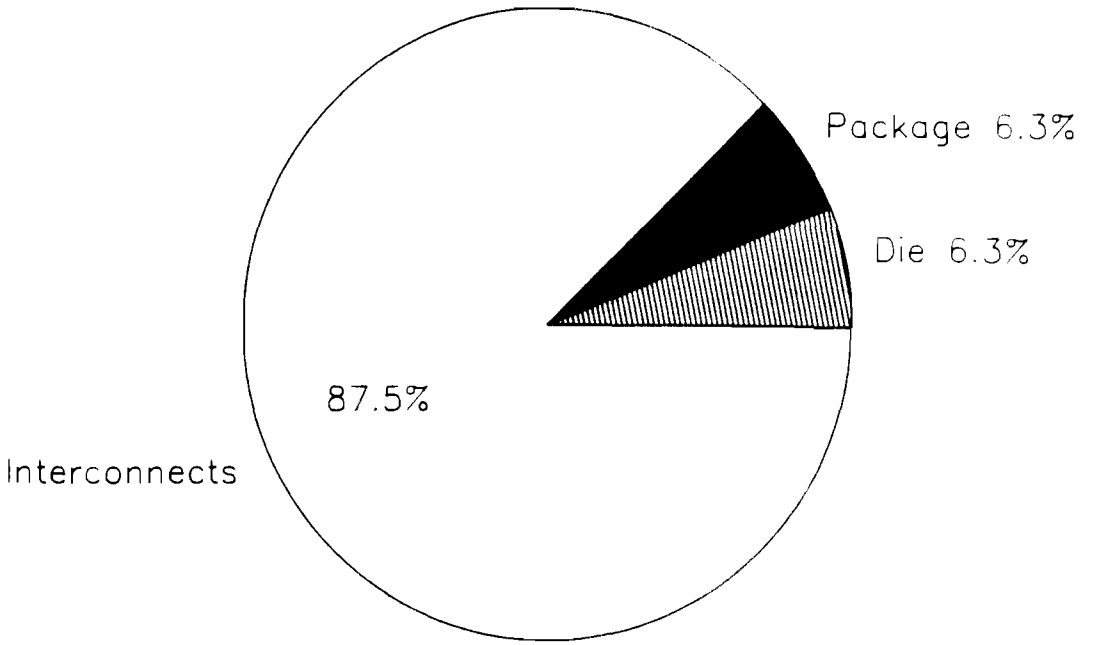


FIGURE A-12:
FAILURE LOCATION
INTERFACE DEVICES

Hermetic Flatpack



Hermetic Chip Carrier

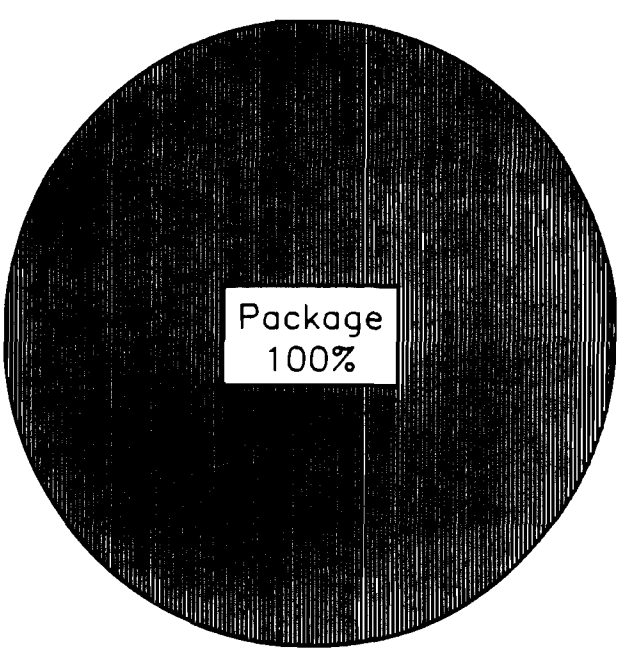


FIGURE A-13:
FAILURE LOCATION
MEMORY DEVICES

Hermetic Flatpack

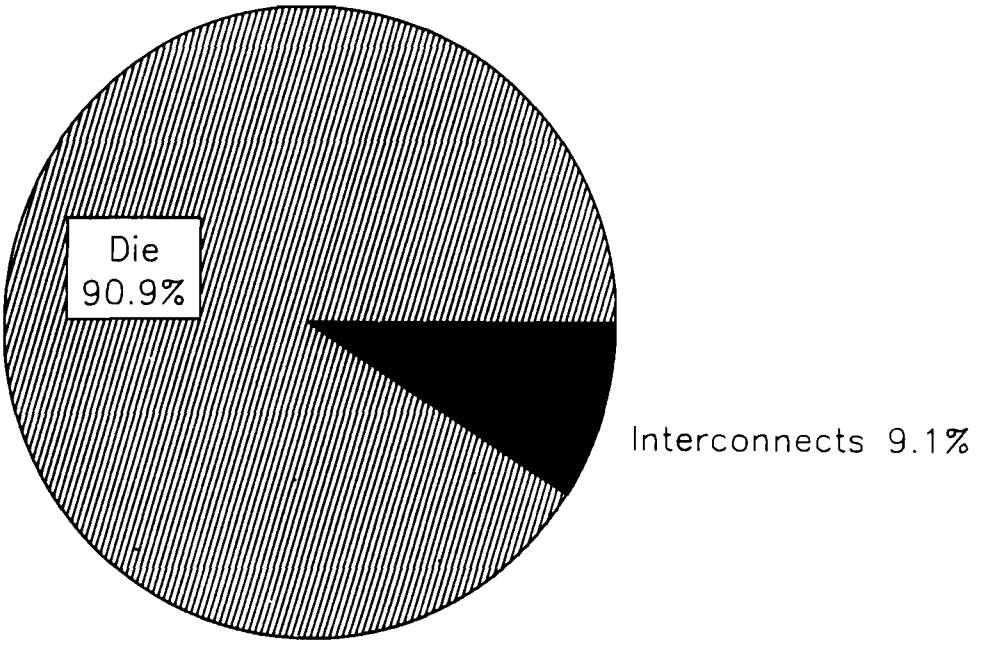


FIGURE A-14:
FAILURE LOCATION
DIGITAL LSI DEVICES

Hermetic Chip Carrier

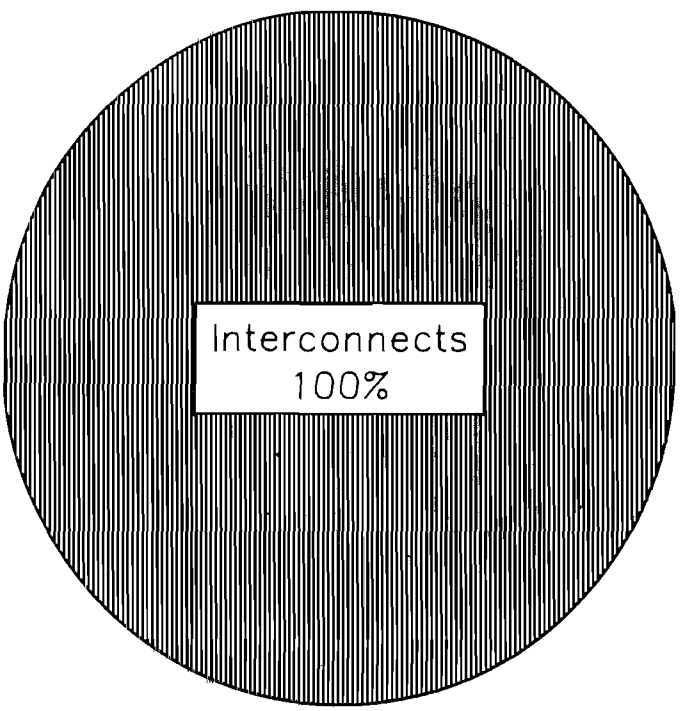
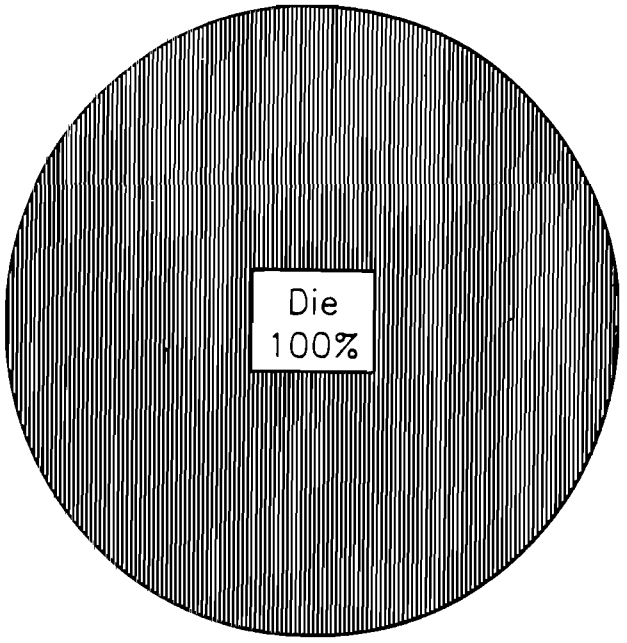


FIGURE A-15:
FAILURE LOCATION
VLSI DEVICES

Nonhermetic Flatpack



Nonhermetic Chip Carrier

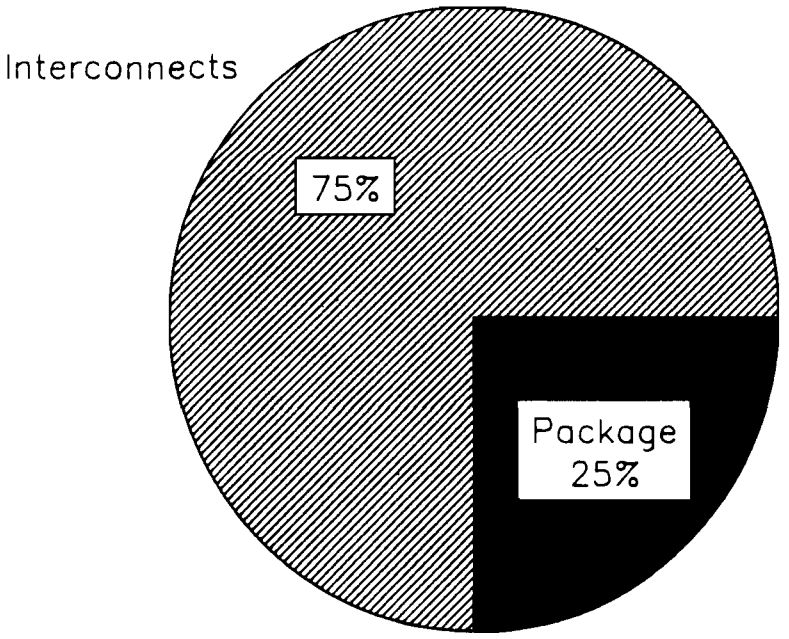


FIGURE A-16:
FAILURE LOCATION
VLSI DEVICES

APPENDIX B:

SMT FIELD AND LIFE TEST DATA

This appendix contains life test and field failure information on Flat Pack and Chip Carrier Devices which is currently available on the Reliability Analysis Center's Integrated Data Base System.

The data output format was developed to be concise and yet informative, consequently, abbreviations are used throughout the report. Various tables and brief descriptions of the abbreviated terms are provided as a guide for interpreting the data.

PACKAGE CONSTRUCTION

Only Flat Pack (FK) and Chip Carriers (CC) data are reported.

SOURCE

Source identifies the basic conditions under which the data were obtained. See Table B-1 for source descriptions.

ENVIRONMENT

The environment defines the area of equipment use. Table B-2 lists the application environments which may be found in this report.

Note: Application Environment is identified only for field data.

CIRCUIT TYPE

Circuit type describes basic circuit function.

PART NUMBER

Component part number.

CLS (SCREEN CLASS)

Screen class distinctions are made based on the testing requirements and level of quality control to which a device is subjected prior to being placed in a working environment. See Table B-3.

IMPLEMENTATION

Fabrication technology from which the device is constructed. See Table B-4.

PINS

Number of package pins.

COMP. (COMPLEXITY)

The complexity factor, given as a numeric, represents a count of the transistors, gates or bits contained within the device. Complexities of devices are specified in the following ways:

Digital = Number of Gates
Linear = Number of Transistors
Interface = Number of Transistors
Memory = Number of Bits

PACKAGE

Device package materials and enclosure mediums are represented here. The package materials are given in Table B-5 and within the parenthesis the package enclosure is identified as one of the following:

(NR) Not Reported
(H) Hermetic
(NH) Non Hermetic

THETA-JC

The junction to case thermal resistance or thermal coeficient of expansion is given in degrees C/Watt.

SDATE/EDATE

The test duration is presented as the start date and end date (last two digits of year and month).

TEST-TYPE

The test-type specifies the test procedures to which a component was subjected. Table B-6 exemplifies the possible stresses associated with each test-type, however, the data contained in this report does not include stress information.

NOTE: A new table is presented for all available combinations of SOURCE, ENVIRONMENT AND CIRCUIT TYPE.

TABLE B-1:

AVAILABLE SOURCES

ABBREVIATION	DESCRIPTION
N.R.	Not Reported
Life	Device Life Test (>=250 Hrs.)
Brn	Device Burn-In Test (<250 Hrs.)
Env	Device Environmental Test
Chk	Equipment Check (Before Rel Demo)
Rel Demo	Reliability Demonstration (Before Production)
Fld	Field Experience
Step	Step Stress (Temp, Pwr or G's only)
Env/Brn	Device Environmental and Burn-In
Bd/Brn	Board Burn-In Test (<250 Hrs.)
Bd/Env	Board Environmental
Eq/Env	Equipment Environmental
Rel/Pro	Reliability Production (Sample Equip. Test After Production)

NOTES:

1) Accelerated Life (above 150 degrees C) is always Life
2) Devices in non-biased tests of less that 250 hours duration will be Env.
3) Env/Brn is to be used when the same parts have been subjected to environmental and burn-in test in sequence (such as screening)

TABLE B-2:
AVAILABLE APPLICATION ENVIRONMENTS

ABBR	DESCRIPTIONS
AA	Airborne Attack
AB	Airborne Bomber
AC	Airborne Cargo
AF	Airborne Fighter
AI	Airborne Inhabited
AIA	Airborne Inhabited Attack
AIB	Airborne Inhabited Bomber
AIC	Airborne Inhabited Cargo
AIF	Airborne Inhabited Fighter
AIT	Airborne Inhabited Trainer
AIU	Airborne Inhabited/Uninhabited
ARW	Airborne Rotary Wing
AT	Airborne Trainer
AU	Airborne Uninhabited
AUA	Airborne Uninhabited Attack
AUB	Airborne Uninhabited Bomber
AUC	Airborne Uninhabited Cargo
AUF	Airborne Uninhabited Fighter
AUT	Airborne Uninhabited Trainer
CL	Cannon Launch
GBC	Ground Benign (Commercial)
GB	Ground Benign (Military)
GF	Ground Fixed
GM	Ground Mobile (Inhabited)
GMU	Ground Mobile (Uninhabited)
GP	Ground Portable
GT	Ground Transportable
MP	Manpack
MFA	Missile Flight Airbreathing
MFF	Missile Free Flight
MSG	Missile Ground Benign
ML	Missile Launch
NH	Naval Hydrofoil
NSS	Naval Sub/Surface Sheltered
NUS	Naval Sub/Surface Unsheltered
NS	Naval Surface Sheltered
NU	Naval Surface Unsheltered
NSB	Naval Undersea Sheltered
NUU	Naval Undersea Unsheltered
N/R	Not Reported
SR	See Remarks
SF	Space Flight
USL	Undersea Launch

TABLE B-3:
AVAILABLE SCREEN CLASSES

ABBR	DESCRIPTION
B	38510 Class B
B-0	38510 Class B (Generic)
B-1	883 Method 5004, Class B
B-2	883 Class B With Waivers
C	38510 Class C
C-1	883 Method 5004, Class C
D	Normal Vendor QC (H-PKG)
D-1	Normal Vendor QC(N-H PKG)
S	38510 Class S

TABLE B-4:

AVAILABLE BASIC IMPLEMENTATIONS

NAME
Not Reported
Bipolar (NOC)
Bipolar, SUHL
Bipolar, TTL
Bipolar, HTTL
Bipolar, LTTL
Bipolar, LSTTL
Bipolar, STTL
Bipolar, ASTL
Bipolar, ALSTL
Bipolar, SUHL
Bipolar, ECL (CML)
Bipolar, ECL High Speed
Bipolar, DTL
Bipolar, RTL
Bipolar, IIL (MTL)
Bipolar, HiNIL
MOS (NOC)
NMOS
NMOS, High Speed
NMOS, Low Power
NMOS, Si Gate
NMOS, Metal Gate
CMOS
CMOS, High Speed
CMOS, Low Power
CMOS, Si Gate
CMOS, Metal Gate
CMOS, SOS
PMOS
PMOS, Si Gate
PMOS, Metal Gate
DMOS
VMOS
MNOS
MESFET
CCD
Bipolar/FET
Bipolar/CMOS
Bipolar/NMOS
Bipolar/PMOS
Bipolar/JFET
Other
Bubble Memory

TABLE B-5:

AVAILABLE PACKAGE MATERIALS

NAME
N/R
Metal
Ceramic
Metal/Ceramic
Metal/Glass
Glass
Plastic/Ceramic
Ceramic/Window
Ceramic/Metal/Window
Epoxy
Ceramic/Plastic/Window
Metal/Epoxy
Silicone
Phenolic

TABLE B-6:

AVAILABLE TEST TYPES

NAME	STRESS A	STRESS B	STRESS C	STRESS D
Not Reported				
Dynamic Characteristics (AC-EM)	Temp (C)			
Constant Acceleration	Force (KG)	# Axes	Time (Min)	
Fine Leak	HE or RADIS	X.E-N,Lk. Rate	T1/Soak (Min)	T2(Min)/P(Atmo)
Gross Leak	Fluor or MinOil	Temp (C)	Mag. (3X)	Pressure (PSIG)
Hermeticity				
High Pressure	Pressure (PSIG)	Temp (C)		
Dew Point				
Immersion	Low Temp (C)	Hi Temp (C)	#CY + Emrs(Min)	Type Liquid
Low Pressure	Vacuum/Atmo	Temp (C)		
Mechanical Shock	Force (G)	Time (M Sec)	# Axes	# Blos
Stabilization Bake	Temp (C)			
Moisture	Low Temp (C)	Hi Temp (C)	%RH	
Radiation Exposure	Free Form			
Salt Atmosphere	Temp (C)	#GMS	Vol M Squared	Time (Hrs)
Salt Spray	Temp (C)	NACL	Time (Hrs)	
Solderability	Temp (C)	%Adherence	Dwell Time(Sec)	
Solder Heat	Temp (C)	Dwell Time		
Static Characteristics (DC-EM)	Temp (C) Note 1			
Operate Equipment				
Temp Cycle	Low Temp (C)	Hi Temp (C)	# Cycles	Dwell Time
Terminal Strength	Weight (oz)	Torque (Degs)	# Arcs	
Thermal Shock	Low Temp (C)	Hi Temp (C)	# Cycles	Liquid or Air
Vibration Fatigue	Frequency (HZ)	Force (G)	# Axes	
Vibration Random	Min Freq (HZ)	Max Freq (HZ)	Force (G)	# Axes
Vibration Variable Frequency	Min Freq (HZ)	Max Freq (HZ)	Force (G)	# Axes
X-Ray	Per Spec.			
RF Interference				
Variable Noise	Frequency (HZ)	# Axes	DB Level	
Visual Inspection		Min Mag (#X)	Max Mag (#X)	
Insulation Resistance	Temp (C)	Volts (KV)	Time BD(Min,Sc)	
Lead Fatigue	Weigth (oz)	Torque (Degs)	# Arcs	
Bond Strength	Min Pull (GMS)	# Bonds (BDS)		

TABLE B-6:

AVAILABLE TEST TYPES (CONTINUED)

NAME	STRESS A	STRESS B	STRESS C	STRESS D
Storage Life	Temp (C)	%Pwr Appl (Opt)		
Operation Constant	Temp (C)	%Pwr Appl (Opt)		
Operation Dynamic	Temp (C)	%Pwr Appl (Opt)		
Humidity Life	Temp (C)	%RH		
Accelerated Life Operating (NOC)	Temp (C)	V or P% Applied		
Intermittent Life	Temp (C)	%Pwr Appl (Opt)	#CY & %Ontime	
Reverse Bias	Temp (C)	%Pwr Appl (Opt)		
Ring Counter	Temp (C)	%Pwr Appl (Opt)		
Autoclave	Pressure (PSIG)	Temp (C)	%RH	Time (Hrs)
Mixed Test Type2	Place all	stresses in	remarks.	
Power Cycle And/Or Temp Cycle	Low Temp (C)	Hi Temp (C)	%Pwr Appl (Opt)	Period(per cyc)
Parallel Excitation	Temp (C)	%Pwr Appl (Opt)		
Temp Cycle, Vibration And Power Cycle	Low Temp (C)	Hi Temp (C)	#Cyc-G's-%Pwr	Freq-%of Vib
Humidity Life/Operation Constant (RHOC)	Temp (C)	%RH	%Pwr Appl	
High Temp Vibration, And Power Cycle	Temp (C)		G's %Pwr On	Freq-% of Vib
Humidity Life/Reverse Bias (RHRB)	Temp (C)	%RH	%Pwr Applied	
Static & Dynamic Characteristics (EM)	Temp (C) Note 1			
EM (NOC)	Temp (C) Note 1			
Burn-In No Stress Specified (NOC)	Temp (C)			
Functional (EM)	Temp (C) Note 1			
Continuity	Temp (C)			
Freeze Out	Low Temp (C)	Hi Temp (C)	T1 (Hr)/T2 (Hr)	T3 (Hr)/T4 (Hr)
Static & Functional (EM)	Temp (C) Note 1			
Dynamic & Functional (EM)	Temp (C) Note 1			
Dynamic, Static & Functional (EM)	Temp (C) Note 1			
Wear Out Life	Temp (C)	Amplitude (V)	Pulse Width(TP)	Rise Time (TR)
Operation Dynamic & High Temp Reverse Bias	Temp (C)	%Pwr Appl (Opt)		
Low Temp, Vibration & Power Cycle	Temp (C)		G's & %Pwr On	Freq(HZ) & %Vib
Rain	Wind Vel (MPH)		Duration(Min)	
Sunshine	Low Temp (C)	Hi Temp (C)	#Cycles/Temp	
Input Protection (CMOS TEST)	Voltage (V)	Capacitance(PF)	Resistance(ohm)	
Accelerated Life/Reverse Bias	Temp (C)	V or P % Appl		
Accelerated Life/Operation Constant	Temp (C)	V or P % Appl		

TABLE B-6:

AVAILABLE TEST TYPES (CONTINUED)

NAME	STRESS A	STRESS B	STRESS C	STRESS D
Accelerated Life/Operation Dynamic	Temp (C)	V or P % Appl		
Operating Life (NOC)	Temp (C)	%Pwr Appl (Opt)		
Tension	Weight (oz)	Time (Sec)		
Accelerated Life/Parallel Excitation	Temp (C)	%Pwr Appl (Opt)		
Thermal Vacuum	Low Temp (C)	Hi Temp (C)	3 Cy (Minimum)	Press (#TORRS)
Thermal Cycle & Power Cycle (1504A)	Low Temp (C)	Hi Temp (C)	24 Cy(Min) %Pwr	#/#DT
Acoustic Noise	Min Frequency	Max Frequency	Max dB Exp Time	
Accelerated Life/Intermittent Life	Temp (C)	%Pwr Appl (Opt)		

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AIF CIRCUIT TYPE : Digital,Array,,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D	CMOS, Metal	16	0	(H)N/R	0	7812/8109	Not Reported	94	0	150,400

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AIF CIRCUIT TYPE : Digital,Discrete,Inverter,Buffer

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D-1	CMOS, Metal	16	6	(NR)N/R	0	7812/8109	Not Reported	94	0	150,400

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : GBC CIRCUIT TYPE : Digital,Array,Gate,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
MCA1200ECL	D	MESFET	68	1,192	(H)Metal/Cera	0	8205/8304	Not Reported	1456	0	1,892,800

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : NS CIRCUIT TYPE : Digital,Decoder,BCD/7-Segment,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	B	Bipolar, LST	20	18	(H)N/R	0	8401/8409	Not Reported	590	4	4,228,530

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AI CIRCUIT TYPE : Digital,,,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D	CMOS, Metal	28	0	(H)Ceramic	0	7812/8109	Not Reported	290	3	261,000

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AI CIRCUIT TYPE : Digital,Counter/Divider,,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
CD4022H	D	CMOS, Metal	16	39	(H)Ceramic	0	7812/8109	Not Reported	290	0	261,000

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AI CIRCUIT TYPE : Digital,Counter/Divider,BCD,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D	CMOS, Metal	48	411	(H)Ceramic	0	7812/8109	Not Reported	290	0	261,000

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AI CIRCUIT TYPE : Digital,Multiplexer,,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D	CMOS, Metal	48	206	(H)Ceramic	0	7812/8109	Not Reported	290	0	261,000

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AI CIRCUIT TYPE : Digital,Miscallaneous,Logic/Process. Unit,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D	CMOS, Metal	48	277	(H)Ceramic	0	7812/8109	Not Reported	290	1	261,000
	D	CMOS, Metal	48	270	(H)Ceramic	0	7812/8109	Not Reported	290	1	261,000

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AI CIRCUIT TYPE : Digital,Discrete,Buffer,Logic Converter

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
CD4049H	D	CMOS, Metal	16	6	(H)Ceramic	0	7812/8109	Not Reported	290	0	261,000

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AI CIRCUIT TYPE : Memory,Register,Shift,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D	CMOS, Metal	48	442	(H)Ceramic	0	7812/8109	Not Reported	290	2	261,000

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : AIF CIRCUIT TYPE : Digital,Counter/Divider,,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D-1	CMOS, Metal	16	39	(NR)N/R	0	7812/8109	Not Reported	94	0	150,400

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : NS CIRCUIT TYPE : Interface,Line/Buss Receiver,,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	B	Bipolar, LST	20	0	(H)N/R	0	8401/8409	Not Reported	490	6	3,511,830

PACKAGE CONSTRUCTION : CC SOURCE : Fld
ENVIRONMENT : NS CIRCUIT TYPE : Memory,PROM,Dynamic,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
5341-2L	B	Bipolar, STT	28	8,192	(H)Metal/Cera	0	8401/8409	Not Reported	281	1	2,013,930

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Not Reported,Not Reported,Not Reported,Not Reported

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
TCC486	D-1	Bipolar, TTL	0	0	(NH)Epoxy	0	/	Humidity Life/Rev	32	0	26,080
TCC486	D-1	Bipolar, TTL	0	0	(NH)Epoxy	0	/	EM (NOC)	32	1	0

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Digital,Miscallaneous,Receiver/Transmitter,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
SN74LS245FN	D-1	Bipolar, LST	20	18	(NH)Epoxy	114	/	Humidity Life	52	0	104,000
SN74LS245FN	D-1	Bipolar, LST	20	18	(NH)Epoxy	114	/	Storage Life	32	0	32,000

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Digital,Miscallaneous,Receiver/Transmitter,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
SN74LS245FN	D-1	Bipolar, LST	20	18	(NH)Epoxy	114	/	Operating Life (N	45	0	0

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Digital,Array,Gate,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	Operation Constan	40	0	43,200
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	EM (NOC)	40	0	0
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	Operation Constan	32	0	34,560
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	EM (NOC)	32	1	0
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	Operation Constan	120	1	119,336
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	EM (NOC)	119	3	0
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	Operation Constan	30	0	32,280
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	EM (NOC)	30	0	0
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	Operation Constan	60	0	60,000
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	EM (NOC)	60	0	0
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	Operation Constan	52	8	51,840
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	EM (NOC)	44	9	0
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	Operation Constan	32	0	23,040
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	EM (NOC)	32	0	0
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	Operation Constan	64	0	21,404
Q700	D	Bipolar, TTL	64	700	(H)Metal/Cera	0	/	EM (NOC)	64	0	0
LL5420AK	D	CMOS, Si Gat	68	4,202	(H)Metal/Cera	0	/8501	Operation Constan	55	0	55,000
LL5420AK	D	CMOS, Si Gat	68	4,202	(H)Metal/Cera	0	/8501	EM (NOC)	55	0	0
LL5080MC	D-1	CMOS, Si Gat	68	880	(NH)Epoxy	0	/8501	Operation Constan	23	0	23,000
LL5080MC	D-1	CMOS, Si Gat	68	880	(NH)Epoxy	0	/8501	EM (NOC)	23	0	0
LL5080MC	D-1	CMOS, Si Gat	68	880	(NH)Epoxy	0	/8501	Humidity Life	24	0	24,000
LL5080MC	D-1	CMOS, Si Gat	68	880	(NH)Epoxy	0	/8501	EM (NOC)	24	0	0
LL5320MC	D-1	CMOS, Si Gat	68	3,192	(NH)Epoxy	0	/8501	Operation Constan	73	0	73,000

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Digital,Array,Gate,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
LL5320MC	D-1	CMOS, Si Gat	68	3,192	(NH)Epoxy	0	/8501	EM (NOC)	73	0	0
LL5320MC	D-1	CMOS, Si Gat	68	3,192	(NH)Epoxy	0	/8501	Humidity Life	52	0	52,000
LL5320MC	D-1	CMOS, Si Gat	68	3,192	(NH)Epoxy	0	/8501	EM (NOC)	52	0	0
LL5140MD	D-1	CMOS, Si Gat	84	1,404	(NH)Epoxy	0	/8501	Operation Constan	12	0	12,000
LL5140MD	D-1	CMOS, Si Gat	84	1,404	(NH)Epoxy	0	/8501	EM (NOC)	12	0	0
LL5140MD	D-1	CMOS, Si Gat	84	1,404	(NH)Epoxy	0	/8501	Humidity Life	18	0	18,000
LL5140MD	D-1	CMOS, Si Gat	84	1,404	(NH)Epoxy	0	/8501	EM (NOC)	18	0	0
LC10000MC	D-1	CMOS, Si Gat	68	1,000	(NH)Epoxy	0	/8501	Operation Constan	154	0	154,000
LC10000MC	D-1	CMOS, Si Gat	68	1,000	(NH)Epoxy	0	/8501	EM (NOC)	154	0	0
LC17800MC	D-1	CMOS, Si Gat	68	1,782	(NH)Epoxy	0	/8501	Operation Constan	31	0	31,000
LC17800MC	D-1	CMOS, Si Gat	68	1,782	(NH)Epoxy	0	/8501	EM (NOC)	31	0	0

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Digital,Discrete,Gate,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
7486	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	Humidity Life/Rev	101	0	68,160
7486	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	EM (NOC)	101	14	0
7486	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	Humidity Life	32	0	34,080
7486	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	EM (NOC)	32	3	0
TCC7486	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	Humidity Life	16	0	26,080
TCC7486	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	EM (NOC)	16	0	0
7408	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	Humidity Life/Rev	80	0	68,160
7408	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	EM (NOC)	80	7	0
SN7408N	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	Humidity Life/Rev	96	0	60,160
SN7408N	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	EM (NOC)	96	3	0
SN7408N	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	Humidity Life	16	0	26,080
SN7408N	D-1	Bipolar, TTL	0	4	(NH)Epoxy	0	/	EM (NOC)	16	0	0
	D	CMOS, Metal	20	4	(H)N/R	0	7906/8005	Storage Life	28	0	28,000

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Digital,Discrete,Gate,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
	D	CMOS, Metal	20	4	(H)N/R	0	7906/8005	EM (NOC)	28	0	0

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Memory,EPROM,Static,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
MR2764-45	D	NMOS, Si Gat	32	0	(H)Ceramic	0	/8211	Reverse Bias	77	0	77,000
MR2764-45	D	NMOS, Si Gat	32	0	(H)Ceramic	0	/8211	Dynamic, Static &	77	0	0

PACKAGE CONSTRUCTION : CC SOURCE : Life
ENVIRONMENT : N/R CIRCUIT TYPE : Memory,EEPROM,,

PART NUMBER	CLS	IMPLEMENTATION	PINS	COMP.	PACKAGE	THETA-JC	SDATE/EDATE	TEST-TYPE	#TEST	#FAIL	#HOURS
MR2816	D	NMOS, Si Gat	32	0	(H)Ceramic	0	/8211	Reverse Bias	77	0	77,000
MR2816	D	NMOS, Si Gat	32	0	(H)Ceramic	0	/8211	Dynamic, Static &	77	0	0

APPENDIX C:
ADDITIONAL RAC SERVICES

PRODUCT FEE SCHEDULE - MARCH 1988

		Price Per Copy Domestic	Foreign
	Component Reliability Databooks		
MDR-14	Hybrid Circuit Data - 1980	$60.00	$70.00
DSR-4	Discrete Semiconductor Device Reliability - 1988	100.00	115.00
NPRD-3	Nonelectronic Parts Reliability Data 1985 - (Printed Copy)	80.00	90.00
FNPRD-3	Diskette of NPRD-3 Data (IBM PC Compatible)	125.00	135.00
VZAP-1	Electrostatic Discharge Susceptibility Data - 1983	95.00	105.00
MDR-21	Trend Analysis Databook - 1985	95.00	105.00
MDR-21A	Field Experience Databook - 1985	125.00	135.00
FMDR-21A	Diskette of MDR-21A Data (IBM PC Compatible)	175.00	185.00
MDR-22	Microcircuit Screening Analysis - 1987	125.00	135.00
MDR-22A	Microcircuit Screening Data - 1987	75.00	90.00
NONOP-1	Nonoperating Reliability Data - 1987	150.00	160.00
	Equipment Databooks		
EERD-2	Electronic Equipment Reliability Data - 1986	80.00	95.00
EEMD-1	Electronic Equipment Maintainability Data - 1980	60.00	70.00
	Handbooks		
RDH-376	Reliability Design Handbook	36.00	46.00
MFAT-1	Microelectronics Failure Analysis Techniques Procedural Guide	125.00	135.00
NPS-1	Analysis Techniques for Mechanical Reliability	56.00	66.00
	Products for Personal Computers		
RAC-NRPS	Nonoperating Reliability Prediction Software (Price includes NONOP-1 listed above)	1400.00	1450.00
	State-of-the-Art Reports		
SOAR-2	Practical Statistical Analysis for the Reliability Engineer	36.00	46.00
SOAR-3	IC Quality Grades: Impact on System Reliability and Life Cycle Cost	46.00	56.00
SOAR-4	Confidence Bounds for System Reliability	46.00	56.00
SOAR-5	Surface Mount Technology: A Reliability Review	56.00	66.00
SOAR-6	ESD Control in the Manufacturing Environment	56.00	66.00
	Technical Reliability Studies		
TRS-2	Search and Retrieval Index to IRPS Proceedings - 1968 to 1978	24.00	34.00
TRS-2A	Search and Retrieval Index to IRPS Proceedings - 1979 to 1984	24.00	34.00
TRS-3A	EOS/ESD Technology Abstracts - 1982	36.00	46.00
TRS-4	Search and Retrieval Index to EOS/ESD Proceedings - 1979 to 1984	36.00	46.00
TRS-5	Search and Retrieval Index to ISTFA Proceedings - 1978 to 1985	36.00	46.00
	MRAP/SRAP Annual Subscription		
MRAP/SRAP	Microcircuit Reliability Assessment Program/Semiconductor Assessment Program	125.00	215.00
FMRAP	Diskette of MRAP Data (IBM PC Compatible) (Includes MRAP/SRAP Basic Subscription)	165.00	265.00

ADDITIONAL RAC SERVICES

Literature Searches

Literature Searches are conducted at a flat fee of $50. For best results, please call or write for assistance in formulating your searc question. An extra charge, based on engineering time and costs, will be made for evaluating, extracting or summarizing informatio from the cited references.

Consulting Services - Call for Quote!

Use order form and send payment, (check or money order), payable to **IITRI/RAC.**

RELIABILITY ANALYSIS CENTER

Reliability Analysis Center/IIT Research Institute, P.O. Box 4700, Rome, NY 13440-8200 (315) 330-4151

ORDER FORM

ORDERED BY:

Name: _____

Company: _____

Divison: _____

Street Address: _____

City: _____

State: _____ Zip: _____

Phone: _____ Ext: _____

SHIP TO: (Only if different than ordered by)

Name: _____

Company: _____

Division: _____

Street Address: _____

City: _____

State: _____ Zip: _____

Phone: _____ Ext: _____

QUANTITY	DESCRIPTION	UNIT PRICE	TOTAL COST

PRIORITY HANDLING - SEE INSTRUCTIONS ON BACK . . . . . _____
QUANTITY DISCOUNT - SEE INSTRUCTIONS ON BACK. . . . . _____
TOTAL OF ORDER . . . . . _____

MAKE CHECKS PAYABLE TO IITRI/RAC

RELIABILITY ANALYSIS CENTER

Reliability Analysis Center/IIT Research Institute, P.O. Box 4700, Rome, NY 13440-8200 (315) 330-4151

ORDER FORM

ORDERED BY:

Name: _____

Company: _____

Divison: _____

Street Address: _____

City: _____

State: _____ Zip: _____

Phone: _____ Ext: _____

SHIP TO: (Only if different than ordered by)

Name: _____

Company: _____

Division: _____

Street Address: _____

City: _____

State: _____ Zip: _____

Phone: _____ Ext: _____

QUANTITY	DESCRIPTION	UNIT PRICE	TOTAL COST

PRIORITY HANDLING - SEE INSTRUCTIONS ON BACK . . . . . _____
QUANTITY DISCOUNT - SEE INSTRUCTIONS ON BACK. . . . . _____
TOTAL OF ORDER . . . . . _____

MAKE CHECKS PAYABLE TO IITRI/RAC

ORDERING INFORMATION

Place orders or obtain additional information directly from the Reliability Analysis Center. Clearly specify the publications and services desired. Except for blanket purchase orders, prepayment is required. All foreign orders must be accompanied by a check drawn on a U.S. bank. **Please make checks payable to IITRI/RAC.**

METHODS OF PAYMENT

Military Agencies: Blanket Purchase Agreement, DD Form 1155, may be used for ordering RAC reports and/or services. Please stipulate maximum dollar amount authorized and cutoff date on your order. Also specify services (i.e., publications, search services, etc.) to be provided. **Identify vendor as IIT Research Institute/Reliability Analysis Center.**

Full Service Participating Plan

Services provided to a participating member are:

- Automatic receipt of one (1) copy of each RAC publication issued during the participation period
- Availability of additional copies of each of the above publications at 20% off list price
- Discount on registration fees for RAC-sponsored training courses, seminars, workshops, etc.

The Plan may be opened in two ways:

- Pre-deposit of a minimum amount of $500 U.S., $575 non-U.S., the maximum to be determined by the requestor
- A purchase order for not less than the above amounts with a "not-to-exceed" amount indicated. IITRI/RAC will bill for services and publications on a quarterly basis.

In addition, the participating member may access RAC resources as needed without issuing purchase orders. RAC will maintain the account record of funds expended and furnish an account statement every 3 months or at the customer's request.

Quantity Discounts - are available, when ordering 10 or more copies. For details call or write Gina Nash at the Reliability Analysis Center, P.O. Box 4700, Rome, NY 13440-8200 (315) 330-4151.

Priority Handling - Add $15.00 per book (Non-US) for Air Mail, add $3.00 per book (US) for First Class.

ORDERING INFORMATION

Place orders or obtain additional information directly from the Reliability Analysis Center. Clearly specify the publications and services desired. Except for blanket purchase orders, prepayment is required. All foreign orders must be accompanied by a check drawn on a U.S. bank. **Please make checks payable to IITRI/RAC.**

METHODS OF PAYMENT

Military Agencies: Blanket Purchase Agreement, DD Form 1155, may be used for ordering RAC reports and/or services. Please stipulate maximum dollar amount authorized and cutoff date on your order. Also specify services (i.e., publications, search services, etc.) to be provided. **Identify vendor as IIT Research Institute/Reliability Analysis Center.**

Full Service Participating Plan

Services provided to a participating member are:

- Automatic receipt of one (1) copy of each RAC publication issued during the participation period
- Availability of additional copies of each of the above publications at 20% off list price
- Discount on registration fees for RAC-sponsored training courses, seminars, workshops, etc.

The Plan may be opened in two ways:

- Pre-deposit of a minimum amount of $500 U.S., $575 non-U.S., the maximum to be determined by the requestor
- A purchase order for not less than the above amounts with a "not-to-exceed" amount indicated. IITRI/RAC will bill for services and publications on a quarterly basis.

In addition, the participating member may access RAC resources as needed without issuing purchase orders. RAC will maintain the account record of funds expended and furnish an account statement every 3 months or at the customer's request.

Quantity Discounts - are available, when ordering 10 or more copies. For details call or write Gina Nash at the Reliability Analysis Center, P.O. Box 4700, Rome, NY 13440-8200 (315) 330-4151.

Priority Handling - Add $15.00 per book (Non-US) for Air Mail, add $3.00 per book (US) for First Class.