Signetics

82S126
82S129
1K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either Open collector or Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126 and 82S129 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

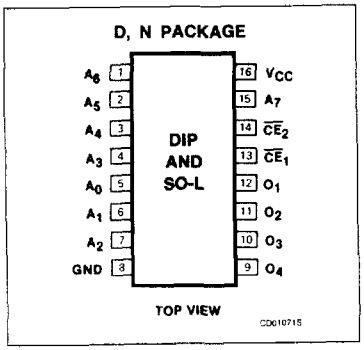
FEATURES

- **Address access time: 50ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Two chip enable inputs**
- **Output options:**
  - **N82S126: Open collector**
  - **N82S129: Three-state**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

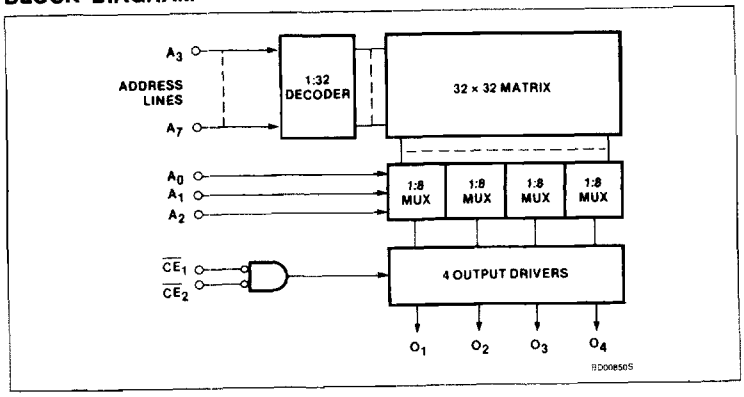
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



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ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S126 N • N82S129 N
Plastic Small Outline 300mil wide 16-pin	N82S126 D • N82S129 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	V_{dc}
V_{IN}	Input voltage	+5.5	V_{dc}
	Output voltage		
V_{OH}	High (82S126)	+5.5	V_{dc}
V_O	Off-state (82S129)	+5.5	
	Temperature range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

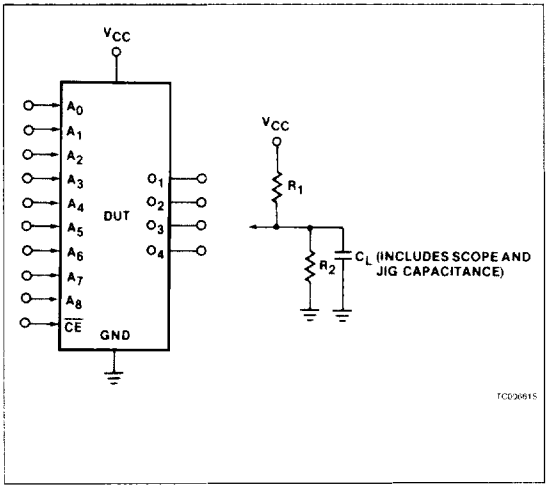
PARAMETER		TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High (82S129)	$I_{OUT} = -2.0mA$	2.4			
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	
Output current						
I_{OLK}	Leakage (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40	μA
I_{OZ}	Hi-Z State (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40	
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit (82S129)[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, Stored High	−15		−70	mA
Supply current						mA
I_{CC}		V_{CC} = 5.25V			120	
Capacitance		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

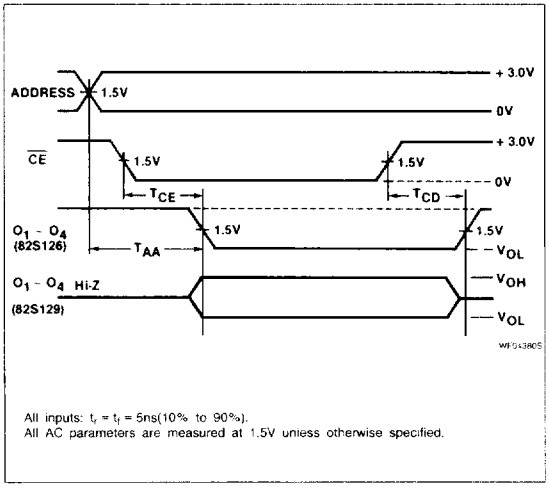
PARAMETER	TO	FROM	MIN	TYP[5]	MAX	UNIT
Access time[4]						
T_{AA}	Output	Address		40	50	ns
T_{CE}	Output	Chip enable			25	
Disable time[6]						
T_{CD}	Output	Chip disable			25	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$(10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

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